

# analog dialogue

A forum for the exchange of circuits, systems, and software for real-world signal processing

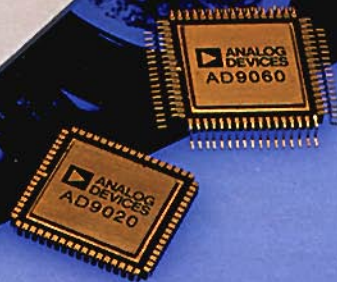
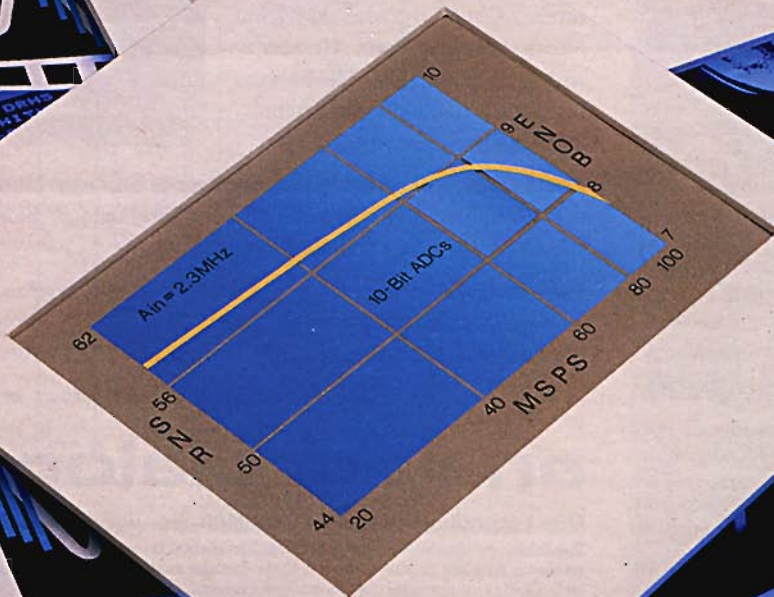
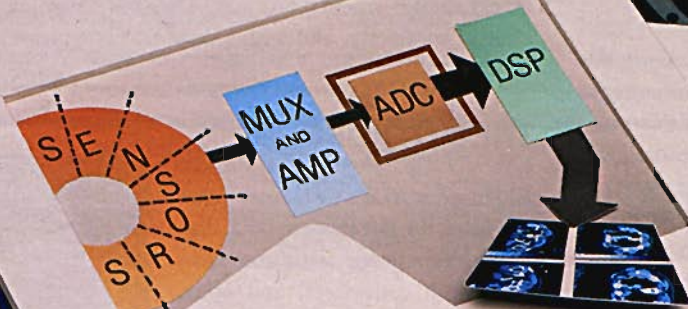
**MONOLITHIC 75-MSPS, 10-BIT FLASH CONVERTER** (page 3)

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# Guest Editor's Notes

## EMPHASIS ON SPEED

This issue of *Analog Dialogue* features the fruits of advanced process technology: two types of devices that can work together in high-speed applications. The ECL 10-bit 75-megasample-per-second AD9060 analog/digital converter (with its TTL version, the 60-MSPS AD9020) is a *monolithic* device that performs better than hybrid- and board-based solutions, with less power dissipation and lower cost.



A high-speed op amp is needed for many jobs. Not the least of its applications is to help realize the full potential of a high-speed converter (such as the AD9020/9060) by serving as a buffer for the input signal. The new pair of current-feedback monolithic op amps, the AD9617 and AD9618, featured in this issue (page 6), are superior choices for this function—and excellent companions for their fellow devices.

It may also be worth a reminder that, to complete the high-frequency analog-digital-analog signal path, the AD9712 and AD9713 DACs (featured in the last issue, 23-4) are optimized for waveform generation.

## NEW IEEE FELLOWS

Two\* long-term contributors at Analog Devices were among the 230 Senior Members elected as Fellows of the transnational Institute of Electrical and Electronics Engineers (IEEE) this year. Dr. Richard S. Payne and Daniel H. Sheingold were accorded the IEEE's highest rank after a rigorous and exhaustive process that required nominators to provide tangible evidence of accomplishments, references from at least five existing Fellows, and recommendations by a Society within IEEE. Election to IEEE Fellow grade is acknowledgment of significant and long term contributions to the state of engineering and its various disciplines and roles. We're honored but not surprised by the choice of these two individuals.

**Richie Payne**, presently Director of the Automotive/Sensors Group at Analog Devices Semiconductor, was cited "for advances in processes for the manufacture of bipolar and CMOS discrete devices and integrated circuits." While at Bell Laboratories, he invented the first successful process for fabricating high-frequency bipolar transistors using ion implantation. It was introduced into manufacturing in 1971 and is still in use.



In his 10 years at Analog Devices, Richie has contributed to and managed process development for high-performance linear, digital, and mixed-signal devices. The strategies and people that he put in

\*In addition to the above, Dr. Joel Moses, Professor of Computer Science and Engineering at the Massachusetts Institute of Technology and member of Analog Devices' Board of Directors, was elected as an IEEE Fellow this year "for leadership in the development of symbolic algebraic manipulation systems."

place have significantly enhanced Analog's leadership position in high-performance analog and mixed-signal process technology.

He also built and managed a major wafer-fabrication facility that puts the results of process development to the severest test: the ability to manufacture and ship advanced ICs in quantity. At present, he is applying this process- and production expertise to the development and marketing of silicon-based sensors, specialized signal conditioners, and advanced sensor interfaces for automotive and other markets.

To many of you, **Dan Sheingold** is the familiar name and face on this page. His formal title "Technical Marketing Manager" obscures many details. As originator, editor, nurturer, and filter of the contents of *Analog Dialogue* for over 20 years, he has provided an ongoing legacy of articles that inform, educate, clarify. His writing and editing in *Analog Dialogue*, in numerous handbooks, and in other technical articles unequivocally disproves the cliché that "engineers can't write."

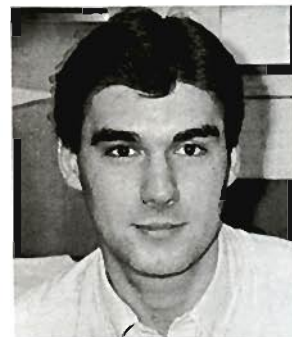


The IEEE citation accompanying his election specifies "for contributions to the understanding and use of analog devices and data converters." When insight into these components and their applications is important (a superior but inadequately described device or capability benefits no one), Dan has shown it can be done clearly, succinctly, and with a style that is a pleasure to read.

Bill Schweber 

## THE AUTHORS

**Chuck Lane** (page 3), a Project Engineer at ADI's Computer Labs Division, in Greensboro NC, has design experience with comparators, flash converters, and other high-speed a/d converter architectures. Chuck graduated from North Carolina State University with a BSEE in 1986. His hobbies include racquetball, table tennis, and reading.



**David Duff** (page 3) is Product Manager in Strategic Marketing at the Computer Labs Division. His photo, and a biographical sketch, appeared in volume 23, number 3.

**Pete Predella** (page 12) is a Technical Publicity Associate at Analog Devices, in Norwood, Massachusetts. His photo, and a biographical sketch, can be found in volume 23, number 3.

(more authors on page 22)

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# FASTEST 10-BIT ADCs PROVIDE SUPERIOR DYNAMIC PERFORMANCE

60-MSPS AD9020 (TTL) and 75-MSPS AD9060 are monolithic devices

Unique LSB interpolating architecture minimizes input capacitance

by Chuck Lane and David Duff

The AD9020 (TTL) and AD9060 (ECL)\* are the fastest monolithic 10-bit analog-to-digital converters available, with respective sampling rates of up to 60 and 75 MSPS. Housed in space-saving 68-pin surface-mount packages, they beat known hybrid and circuit-board solutions in dynamic performance, power consumption, and price. Both devices achieve rated specifications without an input track/hold amplifier; all they require is excitation power, a voltage reference, and a clock to initiate encoding. Applications abound in digital oscilloscopes and instruments, medical imaging, communications, professional video, and in radar systems.

**Architecture:** The AD9020 and AD9060 design<sup>1</sup> (Figure 1) begins with the conventional flash a/d architecture: a string of comparators spaced evenly along a resistor ladder, followed by decoding circuitry which converts the "thermometer-code" output of the comparators into a conventionally coded binary word. Unlike a straightforward 10-bit flash converter design, with  $(2^{10} - 1) = 1,023$  comparators, these devices need only 512. Besides saving real estate, the smaller number of comparators avoids problems of high input capacitance in the 100-pF+ range: difficult to drive at high frequencies—and variations with input voltage cause distortion and degrade dynamic performance.

In the AD9020 and AD9060, an innovative interpolation scheme† halves the number of input comparators (Figure 2a). The 9 most-significant bits are quantized conventionally, but each LSB is determined by combining the outputs of adjacent comparators in interpolating latches. Thus, 512 input comparators have been

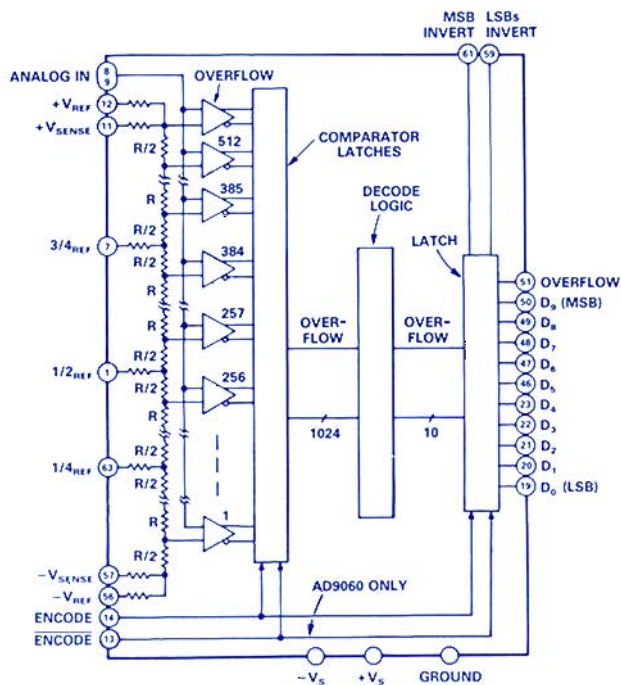
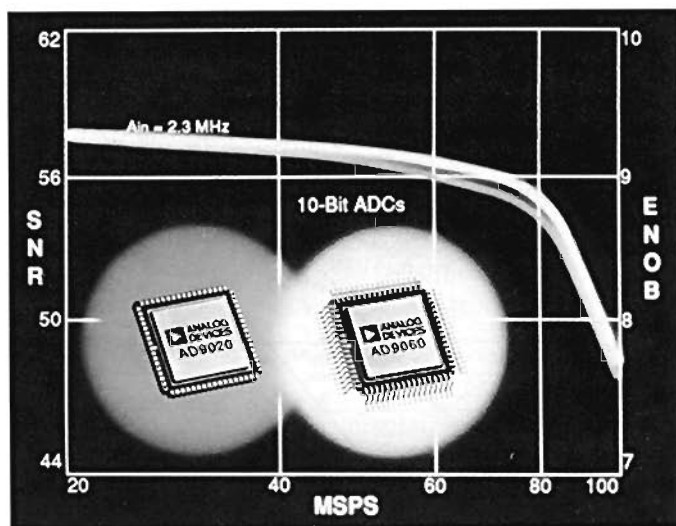


Figure 1. Functional block diagram.

<sup>1</sup>"A 10-Bit 60-MSPS Flash ADC," by Chuck Lane. *Conference Record, IEEE 1989 Bipolar Circuits and Technology Meeting*.

\*Use the reply card for technical data.

†Patent applied for.



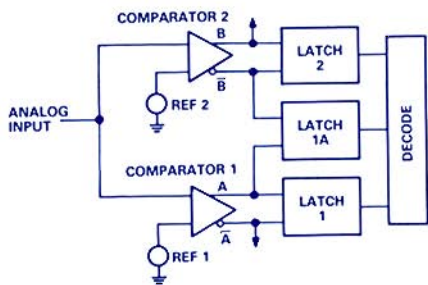
eliminated and replaced by 511 additional differential-input latches, which sum the outputs of the  $m$ th and the  $(n + 1)$ th comparators; but the analog input is not loaded by these latches.

Figure 2b shows the transfer function of the comparators and the effective inputs to the interpolating latches with a linearly increasing input. When the input value is between REF1 and REF2, all comparators below comparator 1 will be saturated, with a high at their non-inverting outputs (to be latched as a binary 1); those above comparator 2 will be in saturation with a high at their inverting outputs (and latched at 0). However, comparators 1 and 2 will be working as amplifiers in the transition region, amplifying the difference between the analog input and the voltage at the associated tap on the reference-divider string.

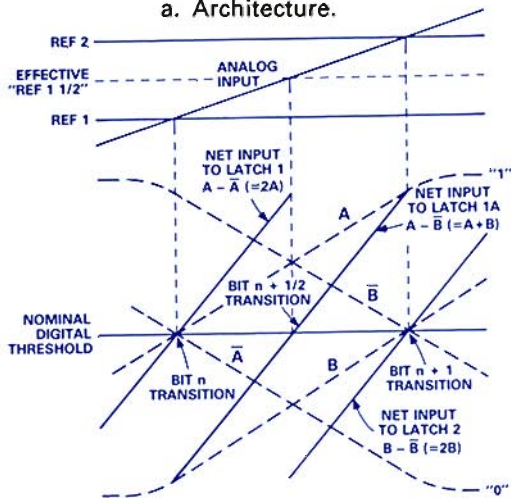
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a. Architecture.



b. Operation. A,  $\bar{A}$ , B,  $\bar{B}$  are the direct and complementary comparator outputs—Note: sums are algebraic, not logical.

Figure 2. Interpolation.

Latch 1A compares the inverting output of comparator 2 ( $\bar{B}$ ) with the noninverting output of comparator 1 (A), producing the sum,  $(A + B)$ ; as the figure shows, the sum crosses the threshold halfway between the transitions of comparators 1 and 2. Latch 1A has a logic 0 output when the input is below this threshold, and 1 above the threshold. Latches 1 and 2 respond to  $(A - \bar{A} = 2A)$ , and  $(B - \bar{B} = 2B)$ , crossing the threshold at the transitions of comparators 1 and 2. Thus latch 1A inserts a bit with a weight of 1/2 the LSB between the bits produced by the comparators. Since latch 1A operates concurrently with latches 1 and 2 to sample the input, there is no pipeline delay between the two sets of bits.

Besides reducing input capacitance, interpolation improves differential nonlinearity (DNL). In traditional flash architectures, a mismatch of 1 LSB between comparators (Figure 3) results in one code appearing two LSBs wide and one code missing (if adjacent comparators are ideal). The interpolation technique doesn't permit this situation to occur, since the code (N - 1) transition is halfway between transitions (N - 2) and N (two 1/2-LSB widths), and the (N + 1) transition is halfway between (N + 2) and N (two 1/2-LSB widths).

**Specifications:** Both ac and dc specs are given because key specifications are application-dependent. *Signal-to-noise ratio* (SNR), for example, is important in radar- and communications-receiver design, since it limits ultimate sensitivity. *Harmonic distortion* measures spurious harmonic signals developed in the a/d converter as a result of device transfer-function imperfections (due to nonlinearities, internal delay mismatch, and varying input impedance). *Two-tone intermodulation distortion* (IMD) results in spurious signals within the passband of a receiver or signal processing system. It is measured as the log power ratio of the the strongest 3rd-order IMD component to either input signal.

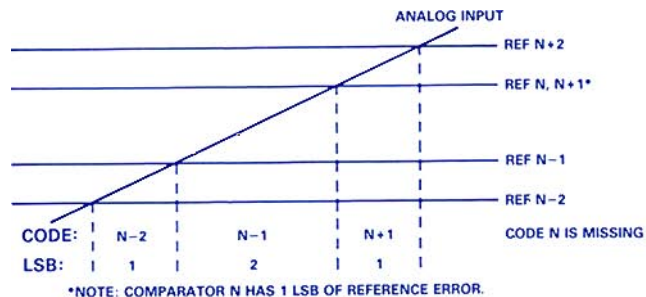
The TTL AD9020 and ECL AD9060 are fully characterized for both static and dynamic input signals, as summarized in the table. Although the converters are specified for encoding rates up to 60 and 75 MSPS, respectively, their performance at other rates and various input frequencies is important to many designers. Figure 4a shows SNR as a function of input frequency; 4b shows effective number of bits (ENOB) as a function of conversion rate. Although maximum conversion rate is defined as the rate above which SNR degradation exceeds 3 dB at low frequencies, the graphs show performance beyond this specified maximum.

### COMPARATIVE SPECIFICATIONS: AD9020 & AD9060

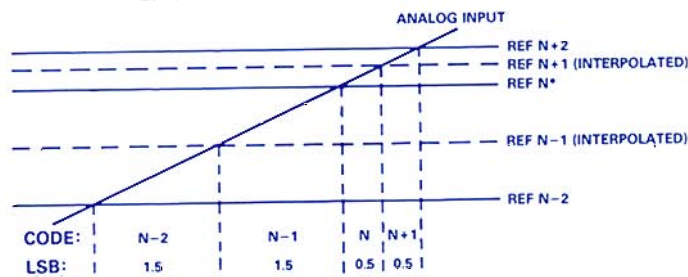
	AD9020	AD9060
Differential nonlinearity (LSB)	1.0	1.0
Integral nonlinearity (LSB)	1.25	1.25
Aperture delay (ns)	1	1
Aperture uncertainty—jitter (ps rms)	5	5
Analog bandwidth (MHz)	175	175
Transient response (ns)	10	10
Overload recovery time (ns)	10	10
ENOB (bits, $f_{in} = 10.3$ MHz)	8.5 @ 40 MSPS	8.5 @ 60 MSPS
SNR (dB, $f_{in} = 10.3$ MHz)	53 @ 40 MSPS	53 @ 60 MSPS
THD (dBc, $f_{in} = 10.3$ MHz)	-59 @ 40 MSPS	-59 @ 60 MSPS
2-tone IMD (dBc, $f_{in} = 10.3$ MHz)	-70 @ 40 MSPS	-70 @ 60 MSPS

**Digital codes:** Conversion is initiated, and the comparators are latched, by the rising edge of the *encode* signal (TTL/CMOS-compatible for the AD9020; ECL-compatible for the AD9060). The 10-bit conversion output is a latched parallel word, in one of four user-selected formats: binary and twos complement—straight or inverted. The format is selected by strapping two control lines to ground or the power rail. An 11th output bit, when high, serves as a flag to indicate that the analog input has exceeded the input range. The overflow bit clears automatically on the next conversion when the input falls below the maximum allowed.

**Voltage reference and performance:** Both devices require user-supplied high- and low voltage references to establish the converter's input range. Applied across the 37- $\Omega$  resistor string, they must be driven from stable, low-impedance sources. Voltage sense



a. With conventional LSB architecture.



b. Improvement due to interpolation.

Figure 3. Comparator offset error.

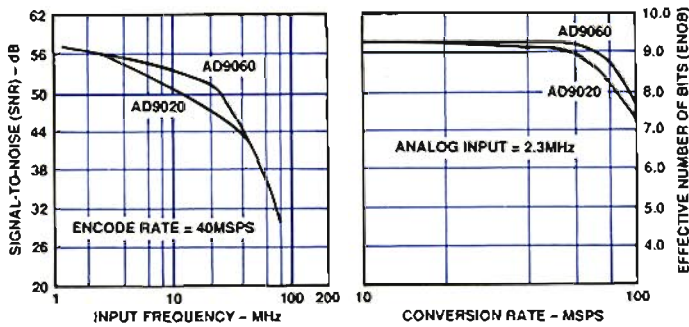


Figure 4. Performance of AD9020 and AD9060. a. vs. input frequency. b. vs. conversion rate.

lines are provided to eliminate offset errors caused by resistance between the external reference and the connections of the first and last comparators to the reference ladder. They permit compensation of the top and bottom ladder offsets; loading of the sense lines should be  $< 100 \mu\text{A}$  to avoid added error.

In addition to the endpoint connections for the reference voltages, there are also mid- and quarter-point ladder taps. These taps can be driven by external sources at 1/4, 1/2, and 3/4 span voltages to achieve the stated integral linearity of the converter (Figure 5). They can be optionally ignored if relaxed specs are permissible. Alternatively, the integral nonlinearity of a particular device can be measured and then partially reduced by adjusting the voltages at the quarter point taps, to improve low-frequency performance.

**Analog input:** The AD9020 and AD9060 are optimized for  $\pm 1.75\text{-V}$  references and analog input range. For smaller spans, the differential nonlinearity will increase because the internal comparator mismatch is larger relative to the LSB. For example, a test resulting in 9 effective bits and 56-dB SNR with a  $\pm 1.75\text{-volt}$  range will decrease to 8.1 effective bits and 51-dB SNR for a  $\pm 0.8\text{-volt}$  range, under otherwise unchanged conditions.

The analog input of the converters presents 7-k $\Omega$  input resistance and 45-pF input capacitance. The input should be driven from a low-distortion, low-noise amplifier such as the AD9617 (this issue, page 6), isolated by a small series resistor (24  $\Omega$  for the AD9617) to improve ac performance of the amplifier.

Evaluation board: Valid evaluation of high-speed flash converters requires careful attention to circuit layout, grounding and ground planes, and stray inductance and capacitance. Evaluation boards are available for both devices (Figure 6), differing principally in accommodations for TTL and ECL. Conversion results, along with a *Data Ready* signal (generated via a delayed clock), are available at a 37-pin connector.

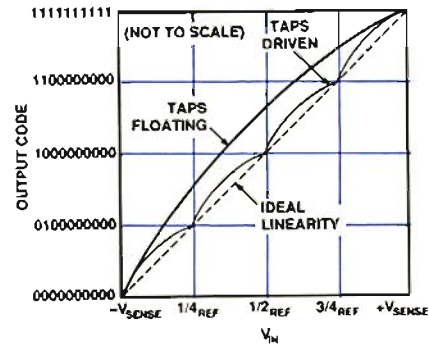


Figure 5. Improvement in integral linearity achieved by driving reference ladder taps.

The evaluation board also incorporates a 12-bit reconstruction DAC to reconvert the digitized values to analog. The DAC allows a quick visual check on performance of the converter (is the device working reasonably well, or are there gross malfunctions?) This is not easily determined by looking at 10-bit words appearing at 60 or 75 MSPS. In addition, the original analog waveform and its reconstructed value (polarity inverted) can be summed to observe qualitatively converter linearity and the effects of adjusting tap voltage or other performance parameters.

The 60-MSPS AD9020 and 75-MSPS AD9060 are packaged in 68-pin leaded and leadless chip carriers. The TTL AD9020 requires a  $\pm 5\text{-volt}$  supply; the ECL AD9060 requires  $+5/-5.2\text{ V}$ . Typical power consumption (both devices) is 2.8 W at 25°C and 3.5 W maximum over the full operating temperature range. Prices (100s) begin at \$165/\$185 for the AD9020/AD9060. ▶

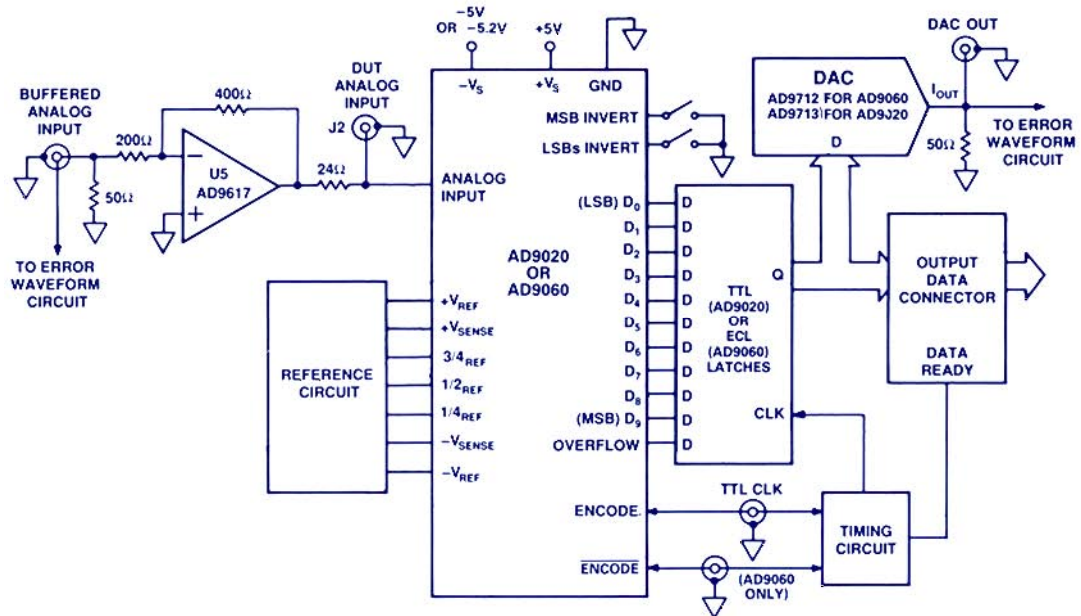


Figure 6. Block diagram of the evaluation board.

# MONOLITHIC OP AMPS HAVE WIDE BANDWIDTH, LOW DISTORTION

Current-feedback AD9617 and AD9618 are optimized for choice of gains

Proprietary architecture offers exceptional dynamic performance

The AD9617\* and AD9618\* monolithic op amps use current feedback and an innovative architecture (patent pending) to provide high speed operation at low cost. The two devices (see Table) are very similar; both have flat wideband closed-loop frequency response and low harmonic distortion, combined with superior dc linearity—commensurate with 16-bit applications.

SPECIFICATION	AD9617	AD9618
Gain Range (V/V)	$\pm 1$ to $\pm 40$	$+5/-1$ to $\pm 100$
Distortion at 20 MHz (2nd h, dBc)	-67	-63
Small-Signal Bandwidth (MHz)	190 ( $A_v = +3$ )	160 ( $A_v = +10$ )
Large-Signal Bandwidth (MHz)	150 (4 V <sub>p-p</sub> )	150 (5 V <sub>p-p</sub> )
Settling time (ns)	9 to 0.1%	
	14 to 0.02%	
Input Offset Voltage (mV)	0.5 typ, 2.2 max	
Input Offset Voltage Drift ( $\mu\text{V}/^\circ\text{C}$ )	3 typ, 10 max	
Input Bias Current, Inverting ( $\mu\text{A}$ )	50 (max)	45 (max)
Output Impedance at dc ( $\Omega$ )	0.07	0.08
Output Current, 50- $\Omega$ Load (mA)	60	60

The op amps differ in their optimal closed-loop gain range: the AD9617 is intended for lower gains—from  $\pm 1$  to  $\pm 15$ —but will provide desirable performance at gains up to  $\pm 40$  V/V; the AD9618 is more suitable for the higher gains up to  $\pm 100$  (but can be used down to gain of  $+5$  and  $-1$ ). The AD9617's second-harmonic distortion spec at 20 MHz is  $-67$  dBc, and it maintains 190-MHz small signal bandwidth at gain of  $+3$  V/V and 150-MHz large-signal bandwidth at 4 V peak-to-peak output. For the AD9618, the corresponding specifications are  $-63$  dBc distortion at 20 MHz, with 160 MHz small signal bandwidth at gain of  $+10$  V/V and 150 MHz large signal bandwidth with 5-V p-p full-scale output.

Applications for these op amps include driving flash a/d converters, such as the AD9020 and AD9060 (see page 3), current-to-voltage conversion of fast d/a-converter outputs, and preamplification stages for photodiodes and CCD sensors. They will be found in instrumentation designs, communications systems, and video processors. The performance of the AD9617 and AD9618 is superior in most respects to hybrid devices, and their 8-pin DIP or small-outline surface mount IC packages save considerable space.

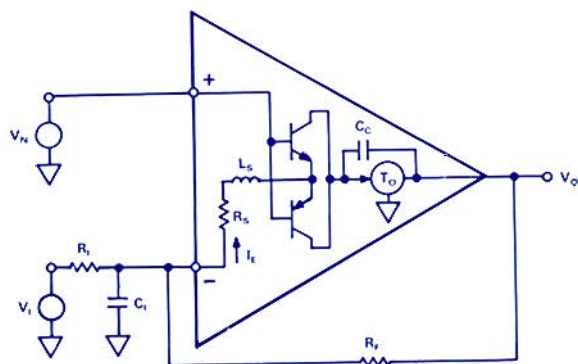
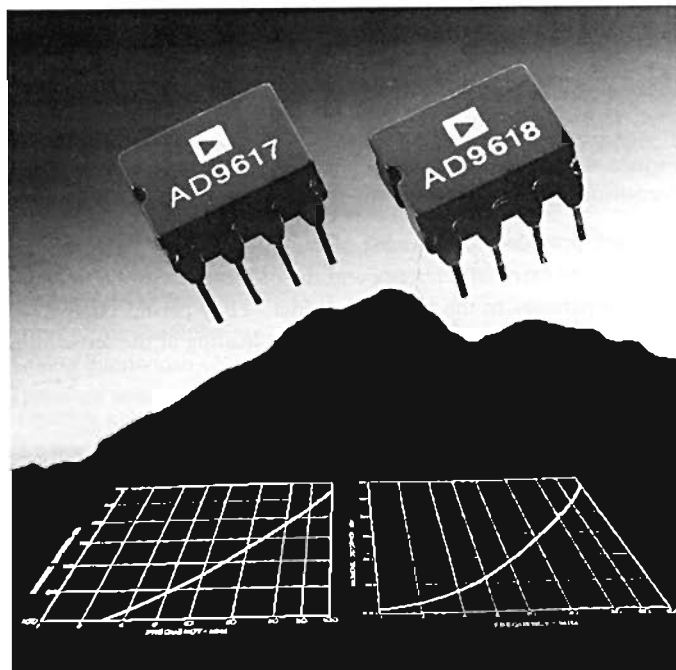


Figure 1. Equivalent circuit.

\*Use the reply card for technical data.



Architecture: Feedback amplifiers (of which operational amplifiers are a subclass) employ two basic types of topology: voltage feedback and current feedback (see "Current Feedback and Transimpedance," *Analog Dialogue* 23-3, page 22). Circuits designed for *voltage feedback* generally have a relatively constant gain-bandwidth product, which forces the closed-loop bandwidth to vary inversely with the closed loop gain. In addition, slew-rate limiting in these amplifiers causes the large-signal bandwidth to be much less than the small-signal value.

*Current feedback*, also used in Analog Devices' op amps such as the AD844 (*Analog Dialogue* 23-2) and AD9610 (*Analog Dialogue* 21-1) provides two advantages over voltage-feedback: slew-rate limiting is avoided, so large signal bandwidth is nearly equal to

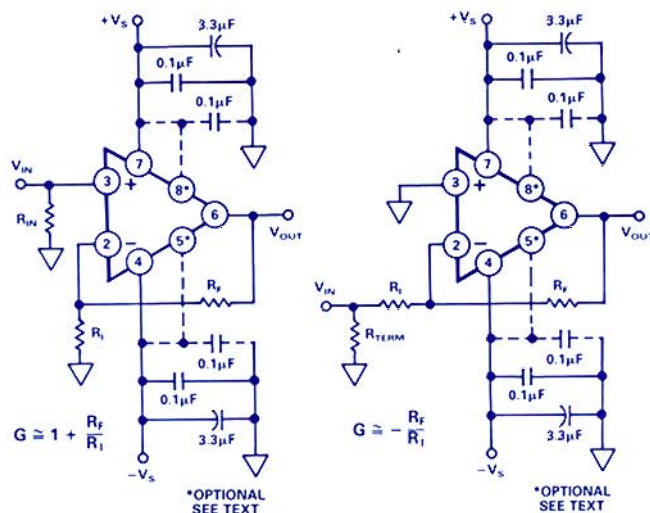
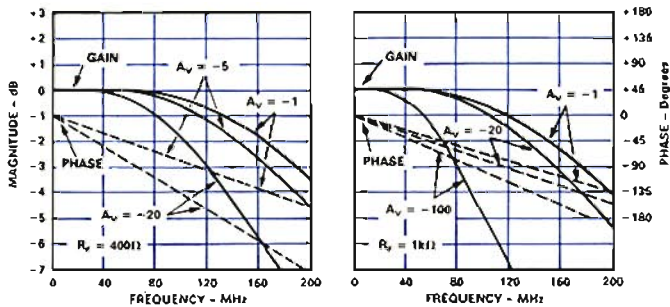


Figure 2. Configurations for noninverting (left) and inverting (right) operation.



a. AD9617. b. AD9618.

Figure 3. Inverting frequency response.

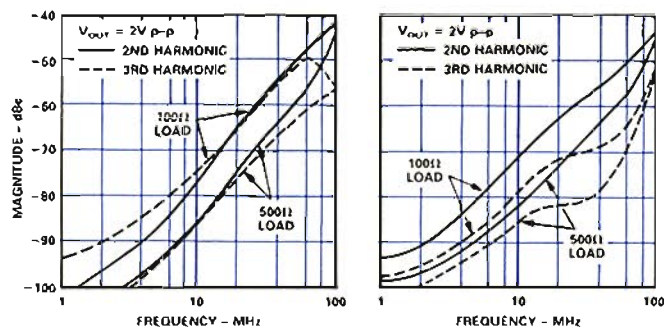
the small-signal value, and bandwidth decreases only slightly as gain is increased (due to the inherently low open-loop inverting input resistance). However, dc performance tends to suffer, because the effective open-loop voltage gain is low compared to that of precision voltage-feedback amplifiers. The consequence is inferior dc linearity and precision, and increased distortion at the higher frequencies (due to open-loop gain rolloff).

The AD9617 and AD9618 are designed to take advantage of the best features of both topologies, while minimizing the drawbacks of each. The result combines the key attributes of lower-frequency precision amplifiers with high frequency characteristics that are independent of the closed-loop gain.

The simplified equivalent circuit (Figure 1), shows basic dc operation and gain. Note that the feedback circuit looks very much like that of voltage-input amplifiers. But in this case, for inverting operation, the input-signal error current ( $I_E$ ) is amplified by the open loop transimpedance gain,  $T_{ov}$ , and the output signal generated is  $T_o \times I_E$ . As in the case of voltage amplifiers, the overall closed-loop gain,  $G$ , is ideally  $-R_F/R_I$ . Figure 2 compares the external circuitry in inverting and non-inverting circuit operation (the dashed-line circuitry can be omitted in an alternate mode of power-supply connection where sockets are already wired for other high-speed op amps).

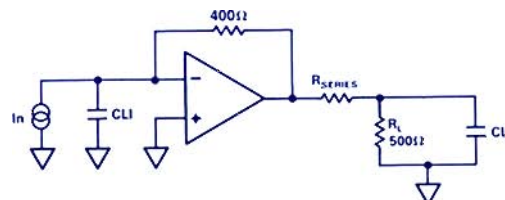
For noninverting operation, the input signal is applied to the high-impedance buffer (noninverting) input. Again, the feedback current,  $I_E$ , is furnished to the low-impedance inverting input; the closed-loop gain is the same as for voltage-input amplifiers,  $(1 + R_F/R_I)$ . The noninverting input should be driven from a low-impedance source to preserve the op amp's full bandwidth.

Closed-loop bandwidth at high frequencies is determined primarily by the rolloff of the transresistance open-loop gain. Although

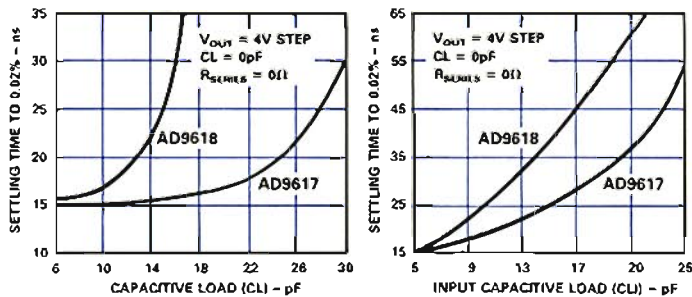


a. AD9617. b. AD9618.

Figure 4. Harmonic distortion.



a. Circuit diagram.



b. Settling time vs. capacitive load

c. Settling time vs. input capacitance.

Figure 5. Capacitive loading test circuit and settling time.

bandwidth does decrease as closed loop gain increases, the change is relatively small because the low equivalent series input impedance (effectively in parallel with  $R_I$ ) maintains an essentially constant ratio to  $R_F$  (see *Analog Dialogue* 21-1, page 22). For low gains,  $R_F$  can be reduced to increase bandwidth and produce faster pulse response, but overshoot and ac peaking may increase settling time.

Layout is, of course, critical at high frequencies. In application, ground planes should be used on the component side of the board in the area of the amplifier, with proper decoupling close to the IC. The pinouts of the AD9617 and AD9618 match industry-standard op amps, so these devices can be retrofitted into existing designs (with appropriate feedback resistance). However, for minimum settling time and lowest distortion, pin 8 should also be connected to  $+V_{S}$ , along with pin 7; similarly, pin 5 should be connected to  $-V_{S}$ , along with pin 4.

**Performance:** The inverting frequency response at a variety of gains for each op amp with  $\pm 5$ -V supplies is shown in Figure 3, with  $R_F$  of 400  $\Omega$  (AD9617) and 1 k $\Omega$  (AD9618). Figure 4 shows the harmonic distortion of each device. Outputs are protected against short circuits to ground.

The output buffer design and low inverting input resistance ( $R_S$ ) allow these devices to drive load capacitances of up to 20 pF (AD9617) and 10 pF (AD9618) directly. For the configuration shown in Figure 5, settling time (to 0.02%) will decrease as indicated for larger loads. To facilitate driving larger capacitive loads (up to 100 pF) or for faster settling time, in applications where dc gain accuracy is not critical, series resistance up to 25  $\Omega$  (outside the feedback loop) can be used to decouple the output.

A commercial-temperature-range ("J"-grade) device is available in an 8-pin plastic miniDIP and SOIC, and two grades of devices for industrial (A,B) and military (S,T) temperature ranges are available in hermetic Cerdip. Quiescent current from each rail of a  $\pm 5$ -V supply is 43 mA maximum. Prices for either op amp begin at \$11.55 (100s).

# A SPICE MACROMODEL OF THE AD9617

Macromodels allow design engineers to simulate electronic components using programs such as SPICE (or its many derivatives). Reasonably accurate models of digital components have been available for several years, but the complexity and subtleties of analog components (in both the linear and non-linear domains) makes models for them more difficult to generate.

Unlike a model based on semiconductor process variables and device geometries, a macromodel uses a simplified equivalent circuit and describes the devices within the circuit by their voltages, currents, parameters, and dependencies. For a design investigation by the user of a macromodel, the complex component (which may have dozens of active and passive devices) is reduced to a multiterminal "black box" behavioral model (represented by the *netlist*) to be interconnected within the final system schematic.

The macromodel listing for the AD9617 is based on the equivalent circuit shown and four basic transistor device models (the model for the AD9618 is nearly identical). The SPICE user of this macromodel calls up a five-terminal device: model node 1 is IC pin 3 ( $V_{in+}$ ); node 2 is pin 2 ( $V_{in-}$ ); node 15 is pin 6 ( $V_{out}$ ); and nodes 100 and 110 are the power rails of pins 7 and 4 respectively ( $V_{CC}$  and  $V_{EE}$ ), paralleled with 8 and 5.

Unlike some macromodels—based on overall specifications or simplified representations—which *oversimplify* by ignoring how the IC is actually built, this model attempts to capture the realities of the analog world. For instance, it emulates the diodes (Q1 and Q2) in the AD9617/AD9618 input stage by using transistors—since that is how these diodes are built. This allows accurate simulation of changes in input circuitry and dc performance with temperature (for example, power supply rejection versus temperature can also be simulated accurately). The graph compares measured and modelled open-loop transimpedance magnitude and phase.

## NETLIST

```
.SUBCKT LGAMP 1 2 15 100 110
* 1 = VIN +, 2 = VIN -, 15 = VOUT, 100 = VCC, 110 = VEE
C1 13 5 1.15P
C2 17 6 1.15P
C3 12 2 0.5P
C4 5 6 3.5P
C5 5 0 1.0P
C6 6 1.0P
C7 12 0 1.5P
CINN 1 0 1.5P
CINI 2 0 1.5P
F1 100 13 VM1 1.5
F2 17 110 VM2 1.5
GM1 12 9 POLY(2) 0 5 0 6 2.5M, -2.0M, -2.0M
GM2 10 12 POLY(2) 0 6 0 5 2.5M, 2.0M, 2.0M
I1 100 3 DC 1.98M
I2 100 5 DC 3.93M
I3 4 110 DC 2.0M
I4 6 110 DC 4.0M
I5 100 12 5.0M
I6 12 110 5.0M
Q1 3 3 1 110 QNA 1.05
Q2 5 3 2 110 QNA 1.05
Q3 4 4 1 100 QPA 1.05
Q4 6 4 2 100 QPA 1.05
Q5 110 12 13 100 QPA 1.25
Q6A 100 13 14 110 QNB 1.05
Q6B 100 13 14 110 QNB 1.05
Q7 100 12 17 110 QNA 1.11
Q8A 110 17 16 100 QPB
Q8B 110 17 16 100 QPB
R1 12 15 500
R2 14 15 5
R3 15 16 5
R4 100 5 190K
R5 5 0 25K
R6 6 110 395K
R7 6 0 12K
R8 7 20 350
R9 12 9 25K
R10 7 8 350
R11 10 12 0.5P
R12 10 12 0.5P
R13 12 9 25K
R14 6 110 4.0M
R15 100 12 5.0M
R16 12 110 5.0M
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# APPLICATION DECIDES OPTIMAL DSP PROCESSOR ARCHITECTURE

## ADSP-2100 family best suited for real-world signal processing Instruction set, arithmetic, data flow, program sequencing are keys

by Bob Fine and David Fair

Selecting an appropriate digital signal processor (DSP) involves many tradeoffs. First, there are traditional engineering factors like cost, memory, speed, programming effort, power consumption. But unlike the selection of an op amp or a/d converter, a DSP's suitability for a given job also involves an aspect more difficult to characterize: the appropriate processor *architecture*. It makes a processor easier to program optimally—a major consideration—and able to accomplish the complete digital signal-processing (DSP) algorithm in less time while requiring less memory and other support.

Real-world DSP applications include digital filters, such as the finite impulse-response (FIR) system modeled in Figure 1, and the decimation-in-time fast Fourier transform, shown schematically in Figure 2; the latter's algorithm flow chart appears in Figure 3. Both applications involve a repetitive pattern of data

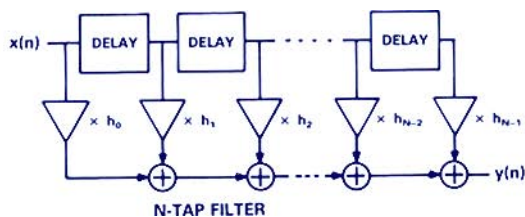


Figure 1. FIR filter principle.

handling and unique symmetries in data structure. To be effective, DSP architectures for processing real-world signals in real time (or at least fast enough to be truly useful) must provide:

- a. *fast and flexible arithmetic*, including single-cycle multiplication (often with accumulation), shifting, and logic operations.
- b. *extended dynamic range on multiply-and-add*—needed for this commonly used DSP function—to protect against overflow, resulting from many successive accumulations.

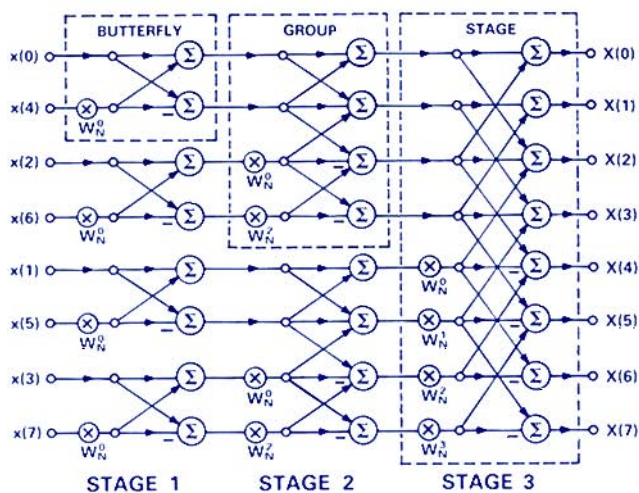


Figure 2. Eight-point decimation-in-time FFT.

\*Use the reply card for technical information.

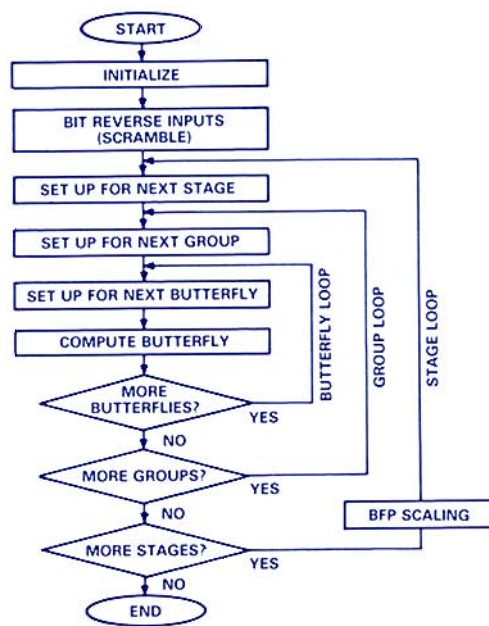


Figure 3. Flow chart for decimation-in-time FFT.

c. *single-cycle fetch of two operands*, as data and coefficient for repeated multiply-and-add calculations.

d. *circular buffering in hardware*, for efficient execution and minimal software burden in address generation for applications such as digital filtering.

e. *looping and branching with zero overhead*: frequently employed DSP algorithms are often inherently repetitive; commonly implemented as program loops, they should execute without undergoing the penalty of extra cycles for checking the end of the loop or for conditional branching out of the loop.

Real-time signal-processing applications are especially critical to three aspects of DSP architecture: *arithmetic processing* (a and b), *data addressing* (c and d), and *program sequencing* (e). The ADSP-2100 family\* of DSP processors is designed with these factors especially optimized for timely signal processing, in contrast to general processing and off-line calculations.

### ARITHMETIC PROCESSING

The arithmetic section of the ADSP-2100 has three computational units (Figure 4)—linked, but independent of one another. The arithmetic/logic unit (ALU), multiplier/accumulator (MAC), and barrel shifter are connected via the R ("results") bus, so that the output of any unit can be used as an input for itself or any other unit on the next cycle. Operands for the ALU and MAC can come from program- or data memory—or specified on-chip registers.

ALU operations can be done on any X-Y pair of the two X and two Y input registers, which in turn can be loaded with data words from any combination of program or data memory buses, or other data registers within the processor. Here's an example of a multifunction ALU instruction combining addition and two

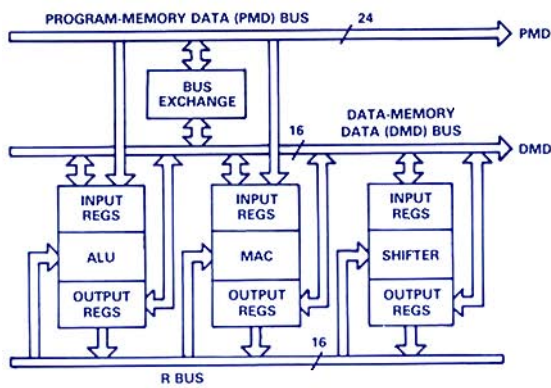


Figure 4. Simplified block diagram of ADSP-2100 arithmetic section.

memory reads (AR is the ALU output register, AX0 and AY1 are two of the ALU input registers):

$$AR = AX0 + AY1, AX0 = DM(I0,M3), AY1 = PM(I4,M7)$$

The first part (up to the first comma) is the addition, the second part loads one X input register with a new operand from data memory, and the third part loads a Y register with a new operand from program memory. The terms in parentheses specify the memory locations to be computed by a pair of address generators. The entire operation is completed in a single cycle (80 ns for a 12.5-MHz-clocked ADSP-2100A).

In contrast, some DSP architectures require one operand to come from the accumulator while the other comes from either the multiplier or from the data bus (via a shifter). When these other architectures are used to add two numbers, the accumulator is first loaded with one data number, then the second number is added to the accumulator—a two-cycle operation. In addition, for this result to be used as an input for anything but another ALU operation, the data must first be transferred from the accumulator to data memory. These restrictions result in a severe arithmetic throughput penalty.

The MAC in the ADSP-2100 performs the complete multiply-and-add operation in one cycle; like the ALU, it has two X and two Y input registers. MAC operands may be loaded from any combination of program memory and data memory, or other processor registers; the MAC feedback and result registers can serve as operands for any MAC operation. Two new operands can be loaded into the input registers during a computation cycle; thus a new MAC operation, with new operands, can start with every cycle (even when accessing off-chip memory).

By comparison, some DSP architectures do not have a multiplier/accumulator as a single entity; the multiplier is separate from the ALU, and the ALU is used for MAC accumulations. A complete MAC operation thus requires two cycles: one to multiply and one to accumulate. The interdependency of ALU and multiplier means that MAC operations cannot be intermingled easily with ALU operations; the order of calculations for the final algorithm may have to be changed to avoid conflicts. In addition to requiring more system time, the instructions for the two-step process require more program memory, in contrast to the multifunction instruction of the ADSP-2100.

The barrel shifter of the ADSP-2100 accepts as input any result register in the processor, including its own result (or its own input register). The shifter can place a 16-bit input value anywhere

within a 32-bit field in a single cycle, and shift any number of input bits from off-scale right to off-scale left. Functions such as exponent detection, normalization and denormalization, and block floating-point manipulation can be realized via this shifter. All shifts, regardless of number of bits to be shifted, are performed in a single cycle.

## DATA ADDRESSING

Fast arithmetic is of course wasted if the required data cannot be fetched at a commensurate speed, regardless of source. To fully utilize the separate data and program memories of the “Harvard” architecture used in most DSPs (in contrast to the single interleaved program/data memory of the Von Neumann computer architecture), the data addressing must support simultaneous dual-operand fetches. The circular buffers often found in DSP algorithms are supported in some DSP processors via built-in address-pointer wraparound; processors lacking this wraparound are at a serious disadvantage in application effectiveness.

The ADSP-2100 has two separate address generators: one typically supplies addresses for data-fetch from program memory (PM) while the other supports data-memory (DM) data fetch. Each address generator’s multiple registers store pointers (addresses), address modifiers, and buffer lengths—for circular (modulo) addressing. For efficient FFT execution, the address generator can reverse (with zero overhead) the order of bits in an address as it is being sent out.

Both indirect and direct addressing are available. In indirect mode, the address *index* register is updated by the contents of a *modify* register, while being put on the bus. The pairing of the various base-address and modify registers is up to the programmer, useful for two-dimensional array addressing or for pointer increment/decrement. The 24-bit-wide instruction word (Figure 5) includes 4 two-bit fields to point to specific PM and DM address registers, plus their respective modify registers.

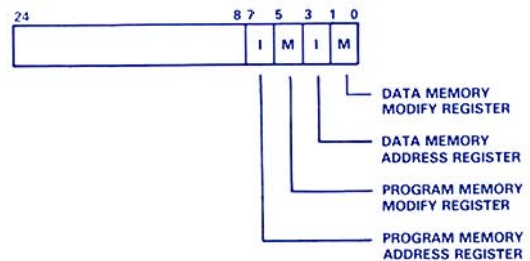


Figure 5. Indirect addressing portion of instruction word

A special *length* register is used for circular addressing. Loading a non-zero buffer length into this register automatically activates the modulus logic. The address and its modulus are maintained transparently by the address generator without explicit calculation by the programmer; and this internal calculation has zero overhead—like many other ADSP-2100 functions.

Some DSPs support both direct and indirect addressing, but with a very limited set of address and modifier registers. This limits flexibility in interleaving several indirect sequences for complex algorithms since the old modify value must be stored and a new one written before the new indirect mode is used. Similar constraints exist for base-address switching.

## PROGRAM SEQUENCING

An efficient DSP for signal processing wastes little or no overhead in maintaining the desired control of data flow. Loops are funda-



# 14-BIT 2-CHANNEL SYNCHRO/RESOLVER-TO-DIGITAL CONVERTER

The AD2S44 features two independent channels and error-detection circuitry, accuracy to within  $\pm 2.6$  arc-min over temperatures from  $-25$  to  $+85^\circ\text{C}$

by Pete Predella

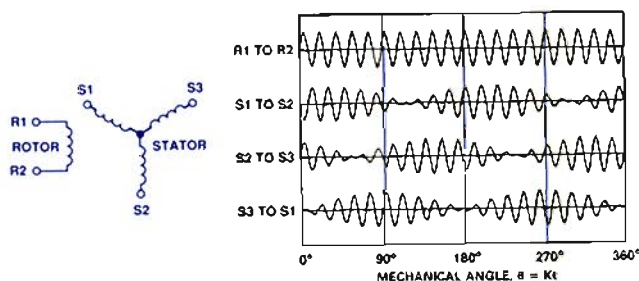
The AD2S44\* is a dual-channel, continuously tracking synchro/resolver-to-digital converter. It can independently accept ac sinusoidal signals from two synchros or two resolvers—using independent references—and convert them to 14-bit digital words that represent angular position. Its maximum error (U grade) is only  $\pm 2.6$  arc-minutes (2 LSB) over temperatures from  $-25$  to  $+85^\circ\text{C}$  (increasing to only  $\pm 4.0$  arc-min from  $-55$  to  $+125^\circ\text{C}$ ), at speeds up to 20 revolutions per second. Housed in a 32-pin hybrid package, the compact AD2S44 offers a low-cost, space-saving solution to dual-axis servo-loop position-control systems.

Electronic systems that measure and/or control the motion of mechanical devices need to determine linear and angular displacements continuously. In many cases, rotations around pairs of orthogonal axes must be measured; examples include radar, gyro compasses, smart munitions, and aircraft and missile control systems. For instance, in order to guide a large missile accurately toward its target, it is necessary to measure the target's azimuth and elevation (by positioning an infrared sensor to track the target), the missile's attitude (relative to two gyroscopically established axes), and the angular positions of the control fins.

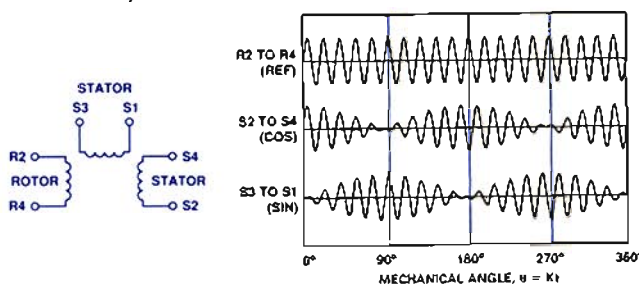
**Synchro and Resolver Input Formats:** The AD2S44 accepts signals in both synchro- (three signals at  $120^\circ$ ) and resolver (two signals  $90^\circ$  apart) formats (Figure 1); they are applied to the converter according to the following convention:

## Synchro Format

$$\begin{aligned} E_{S1-S3} &= E_{RLO-RH1} \sin \omega t \sin \theta \\ E_{S3-S2} &= E_{RLO-RH1} \sin \omega t \sin (\theta - 120^\circ) \\ E_{S2-S1} &= E_{RLO-RH1} \sin \omega t \sin (\theta - 240^\circ) \end{aligned}$$



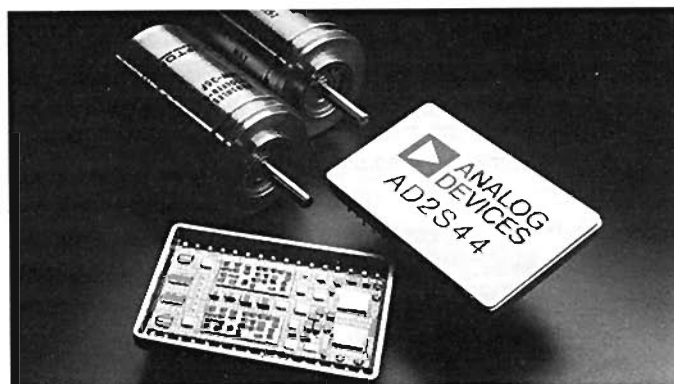
a. Synchro has three windings  $120^\circ$  apart.



b. Resolver has two windings  $90^\circ$  apart.

Figure 1. Synchro and resolver winding wave forms with linearly increasing angle.

\*Use the reply card for technical data.



## Resolver Format

$$\begin{aligned} E_{S1-S3} &= E_{RLO-RH1} \sin \omega t \sin \theta \\ E_{S2-S4} &= E_{RLO-RH1} \sin \omega t \cos \theta \end{aligned}$$

The terminal designations in these equations relate to the connections to the inputs of unit A or unit B in Figure 2.

## RATIOMETRIC CONVERSION

Because angular position information resides in the *ratios* of the magnitudes of the transducer's outputs to one another, the best method to digitize these input signals is a *ratiometric* conversion technique—like that used in the AD2S44—that ignores absolute magnitude. The process involves continuous error-signal integration in a tracking feedback loop, and the converter features high noise immunity, tolerance of harmonic distortion, and common-mode voltage rejection up to 210 volts dc. In addition, sizeable voltage drops (i.e.,  $\pm 10\%$  of FS) in long lead lengths from the transducer to the converter go relatively unnoticed.

When shaft-angle data must be processed at a considerable distance from the transducer, synchros or resolvers are preferred to optical or contact encoders. Data transmitted by an encoder over great distances, sent as either serial pulses or as a parallel word, is susceptible to noise, jitter, interference, and signal transients—leading to false counts. Synchros and resolvers, on the other hand, can transmit analog information over distances up to 2 kilometers, using three- or four-wire twisted-pair shielded cable. The AD2S44 integrates this signal with a high degree of noise immunity, effectively ignoring transients, and can withstand high common mode voltages.

**Input Signal Conditioning:** In the basic signal conversion process (Figure 2) the digital output angle ( $\phi$ ) at the counter output is continuously compared with the synchro/resolver input angle ( $\theta$ ), and the tracking loop acts to null their difference. The input signals are fed directly to a solid-state Scott-T signal conditioner, which serves as a precision attenuator to reduce the amplitude of high-level ac signals to levels the converter can process; this conditioner can eliminate the need for external transformers in many designs because of its high common-mode rejection.

The signal conditioner produces two independent output voltages:

$$\begin{aligned} V_1 &= K E_O \sin \omega t \sin \theta \\ V_2 &= K E_O \sin \omega t \cos \theta \end{aligned}$$

where  $\theta$  is the angle of the synchro/resolver shaft,  $E_o \sin \omega \tau$  is the reference signal, and  $K$  is the scaling constant.  $V_1$  and  $V_2$ , and a feedback angle ( $\phi$ ) from the up/down counter, go to a high-speed multiplier which computes  $V_1 \cos \phi$  and  $V_2 \sin \phi$ :

$$K E_o \sin \omega \tau \sin \theta \cos \phi$$

$$K E_o \sin \omega \tau \cos \theta \sin \phi$$

These signals are then subtracted by an error amplifier; the result is an error voltage ( $e$ ) proportional to  $\sin(\theta - \phi)$ :

$$e = K E_o \sin \omega \tau (\sin \theta \cos \phi - \cos \theta \sin \phi)$$

$$= K E_o \sin \omega \tau \sin(\theta - \phi)$$

The phase-sensitive detector (PSD) generates a dc signal proportional to  $\sin(\theta - \phi)$ . This signal is integrated and fed to the VCO input, which clocks the up-down counter. Once the tracking loop is synchronized, the output angle will track constant-velocity inputs without lag error and the digital output is a direct representation of the shaft angle.

### BUILT-IN TEST

The error voltage signal of both channels is continuously monitored; if either error signal exceeds  $\pm 50$  LSBs (about  $\pm 1^\circ$ ), the converter produces a logic signal ( $\overline{\text{BIT}}$ ) to indicate one or more of the following fault conditions:

- Over velocity—a condition where the maximum tracking rate of 20 rps is exceeded.
- Power up— $\overline{\text{BIT}}$  is active until the converter is synchronized with the input
- Instantaneous step inputs  $> 1^\circ$
- Input signal failure—loss of reference voltage or input signal
- System failures—including excessive acceleration errors, poor supply-voltage regulation, or excessive noise.

$\overline{\text{BIT}}$  is typically valid within 50 ns of a fault occurrence, which must last for at least one period of the reference signal. Reset occurs when the error signal drops below the equivalent of  $\pm 45$  LSBs. The built-in  $\pm 5$ -LSB hysteresis reduces flickering as error thresholds are crossed.

**Input Scaling:** Input signal and reference voltages greater than the converter's 10% signal tolerance can be scaled using external resistors. Because a 0.1% resistor value mismatch will contribute

as much as 1.7 arc minutes of error and reduce the input signal's common-mode rejection ratio, the use of precisely matched (e.g. 0.01%) resistors is recommended.

**Acceleration error:** The acceleration constant,  $K_a$  ( $= 62,000 \text{ s}^{-2}$ ) can be used to define the error due to acceleration as:

$$\text{Error in Output Angle} = \frac{\text{Input Acceleration}}{K_a}$$

$K_a$  can be used to estimate an output position error. The converter can support maximum errors of  $\pm 5^\circ$  without losing track. This implies that the maximum acceleration is  $5^\circ K_a$  ( $= 310,000 \text{ s}^{-2}$  or about 860 revolutions/s<sup>2</sup>). In reality, most mechanical systems couldn't sustain these levels of acceleration without serious destructive consequences. The output position error in LSBs due to acceleration is:

$$\text{Error in LSBs} = \frac{\text{Input acceleration [LSB/s}^2\text{]}}{K_a [\text{s}^{-2}\text{]}}$$

For example, the error for acceleration of 50 rev/s<sup>2</sup> is:

$$= \frac{50 [\text{rev s}^{-2}] \times 214 [\text{LSB/rev}]}{62,000 [\text{s}^{-2}]} = 13.2 \text{ LSB}$$

Therefore, an acceleration of 50 rev/s<sup>2</sup> would not trigger  $\overline{\text{BIT}}$ .

**Maximum tracking rate:** The AD2S44 can track constant-velocity signals at up to 20 rps without error. Although this maximum tracking rate is more than adequate for most applications, the intervention of  $\overline{\text{BIT}}$  is particularly important in fail-safe designs. For example,  $\overline{\text{BIT}}$  can be used to shut down runaway/open-loop servo-control systems.

**Reliability:** Mean time between failures (MTBF) is a calculated measure of a product's reliability, based primarily on its design and operating environment as a function of time (years). Hybrids with few components offer inherently higher MTBF rates than hybrids or discrete designs with many active components. For the AD2S44, the calculated MTBF for Naval Sheltered conditions, in accordance with MIL-HDBK-217E, is  $> 80$  years at a steady  $+25^\circ\text{C}$  case temperature, and 11 years at  $+85^\circ\text{C}$ .

The AD2S44 is available in three accuracy grades, with options for all industry-standard signal and reference-voltage levels. The AD2S44's input reference-frequency range is from 400 Hz to 2.6 kHz. Prices in 100s begin at \$418 (i.e., \$209 per channel).

The AD2S44 was designed by Paul Blacknell, of ADI's Memory Devices Division, in East Molesey (Surrey), England. ▶

### KEY SPECIFICATIONS

Parameters	AD2S44	Units	Comments
Resolution	14	Bits	Natural Binary
(1 LSB = 1.3 arc min)			
Accuracy: Max Error			
AD2S44UM	$\pm 4$	arc-min	$-55$ to $+125^\circ\text{C}$
AD2S44TM	$\pm 2.6$	arc-min	$-25$ to $+85^\circ\text{C}$
AD2S44SM	$\pm 5.2$	arc-min	$-55$ to $+125^\circ\text{C}$
Tracking Rate	20	rev/s	
Acceleration Constant	62,000	$\text{s}^{-2}$	
Repeatability	1	LSB	
Bandwidth	100	Hz	
Min CMR	74	dB	
Step Response			
179°	75	ms, max	To $< 1$ LSB
2°	30	ms, max	To $< 1$ LSB

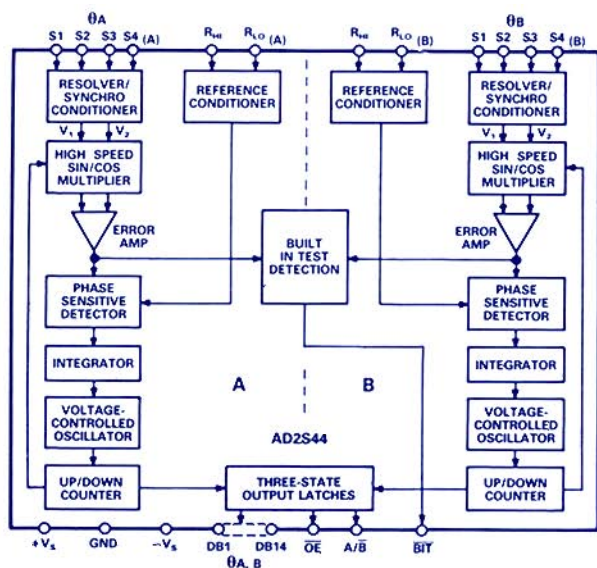


Figure 2. Block diagram of the AD2S44.

# 12-BIT, 100-KSPS COMPLETE SAMPLING A/D CONVERTERS

Monolithic AD7875, AD7876 have 0 to +5-V,  $\pm 10$ -V input ranges

Footprint, serial and parallel outputs: same as  $\pm 3$ -volt-input AD7870

The AD7875 and AD7876\* use a high-density linear-compatible bipolar/CMOS process (LC<sup>2</sup>MOS) to combine a 12-bit a/d converter (ADC), sample/hold (SHA), reference, and interface logic on a single monolithic chip. Their high dc accuracy and high conversion rate (100 ksp/s with a 2.5-MHz clock), are useful in high-speed traditional measurement-and-control applications—especially where large numbers of channels are multiplexed—formerly requiring a separate SHA and ADC. In addition, the AD7875's dynamic specifications are useful in spectrum analysis, speech processing, and telecommunications.

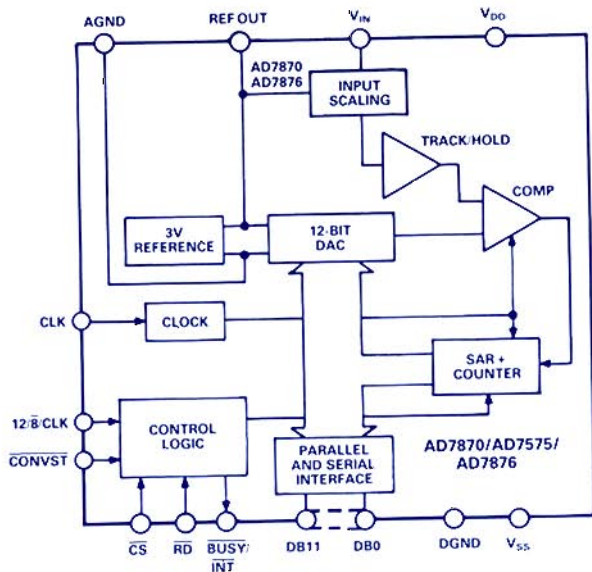
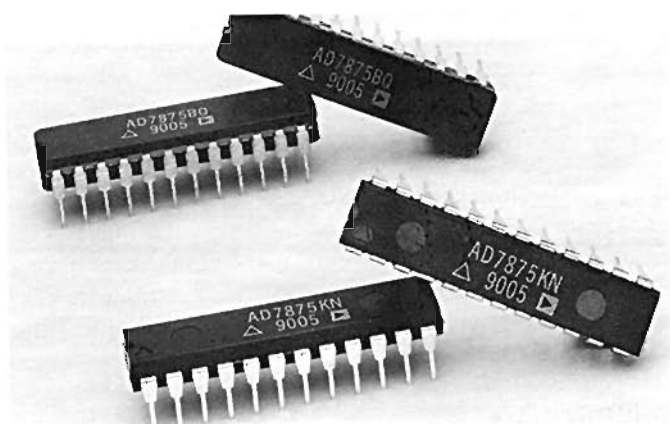


Figure 1. Block diagram.

Both devices (Figure 1) have a track-hold amplifier with 2- $\mu$ s acquisition time, a 12-bit a/d converter with 8- $\mu$ s conversion time, a 3-volt on-chip precision reference, a laser-trimmed clock, and a versatile interface capable of communicating in parallel, byte-

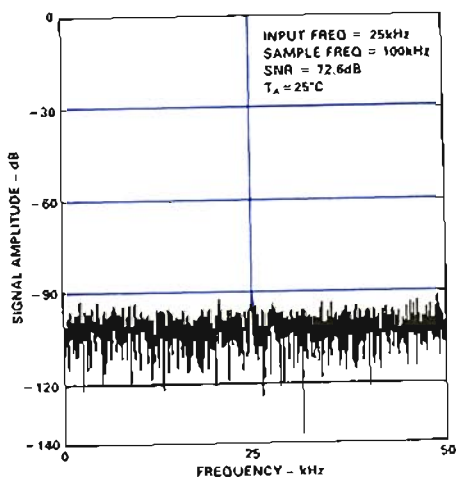


Figure 2. FFT plot for AD7875KN with 25-kHz input signal sampled at 100 kHz.

\*Use the reply card for technical data.

serial, and bit-serial. The interface's 57-ns data-access time makes these devices compatible with modern 8- and 16-bit microprocessors and digital signal-processors.

Both units guarantee no missing codes at 12-bit resolution for all grades over the specified temperature ranges. In addition, the premium L and C grades have  $\pm 1/2$ -LSB maximum integral nonlinearity over temperature; this is a useful feature in measurement-and-control applications. They differ principally in input voltage range—0 to +5 volts for the AD7875 and  $\pm 10$  V for the AD7876. On the other hand, the AD7875 is also specified dynamically in terms of ac response: 71-dB minimum signal-to-noise (including distortion) over temperature for the C and L grades, with -80-dB maximum total harmonic distortion and peak spurious response. Figure 2 is a 2,048-point FFT plot of a typical AD7875's response to a 25-kHz sine wave sampled at 100 ksp/s. Note that the peak spurious signal is at about -88 dB; the SNR is computed as 72.6 dB.

These ac specifications are useful in communications, spectrum analysis, and applications involving digital signal processing. Figure 3 shows a serial interface to the ADSP-2101 DSP chip.

Both high-performance devices are available in two grades each for 0 to +70°C (K & L) and -40 to +85°C (B and C), with a "T" (/883B) grade for -55 to +125°C. The extended temperature grades are available in hermetic DIP packages, while the K and L grades have a choice of plastic DIP and PLCC (AD7875) or SOIC (AD7876). Prices begin at \$20.00 (100s).

The AD7875 and AD7876 were designed by Ray Speer at Analog Devices BV, in Limerick, Ireland. ▣

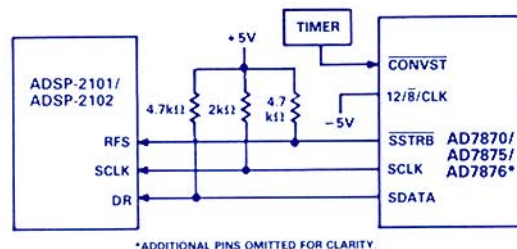


Figure 3. Serial interface to ADSP-2101 single-chip Digital Signal Processor.

# ISOLATION AMPLIFIER FOR LOW-LEVEL SIGNALS

High-precision AD208B has 1.5-kV rms isolation, 1-to-1,000 V/V gain range  
Combines 0.0125% nonlinearity,  $\pm 1.5 \mu\text{V}/^\circ\text{C}$  max drift,  $-40$  to  $+85^\circ\text{C}$

The AD208\* is a high-precision two-port transformer-coupled dc isolation amplifier designed for millivolt-level applications requiring signal isolation, high common-mode rejection and linearity, wide gain range, and low drift. It is packaged in a compact  $2.08'' \times 0.26'' \times 0.625''$  plastic single in-line package.

Applications abound in instrumentation and process-control measurements, especially in the isolation and precise amplifying of signals from thermocouples and RTDs. The AD208 is also useful as a general-purpose isolated front end for inputs to measurement systems requiring 12-bit linearity and resolution.

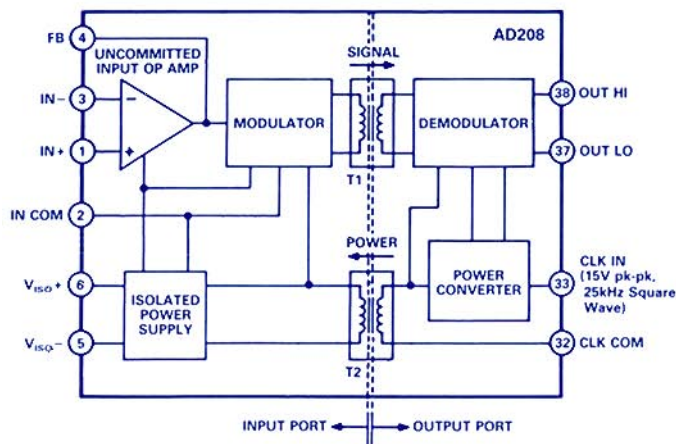


Figure 1. Functional block diagram.

Figure 1 illustrates the physical features of the AD208. Included are: an uncommitted input op amp that can be connected for flexible input functions, including any gain value from 1 to 1,000 V/V; up to  $\pm 8 \text{ V} @ \pm 5 \text{ mA}$  of isolated front-end power for excitation or auxiliaries, e.g., op amps and references; and two-port transformer-coupled isolation of up to 1,500 Vrms, 2,000 V peak ac & dc ("B" grade). Primary power is a 25-kHz 15-volt p-p square wave, furnished by an external clock source, such as the AD246J clock driver. The AD246, available in a SIP "Y" package, can drive as many as 16 fully loaded AD208s.

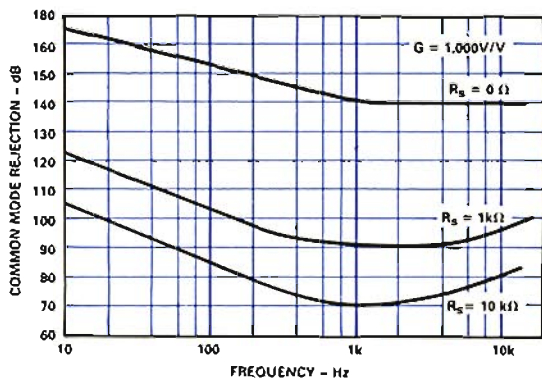
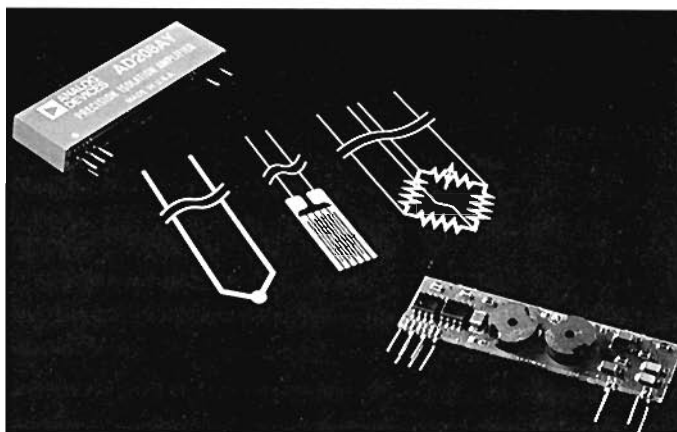


Figure 2. Common-mode rejection as a function of common-mode signal frequency and source imbalance at  $G = 1,000 \text{ V/V}$ .

\*Use the reply card for technical data.



The AD208's performance includes low offset and drift, referred to the input ( $\pm 0.27 \text{ mV max}$ ,  $\pm 1.5 \mu\text{V}/^\circ\text{C max}$  at  $G = 1,000$ ;  $15 \text{ mV}$  and  $22 \mu\text{V}/^\circ\text{C max}$  at  $G = 1$ ); low nonlinearity (0.015% max, "B" grade,  $\pm 5\text{-V}$  output swing); and low gain error and gain drift ( $\pm 2.5\%$  and  $\pm 20 \text{ ppm}/^\circ\text{C}$ , max). Associated with its 1.5 kV of isolation ("B") are common-mode rejection of 100 dB (60 Hz,  $R_s < 1 \text{ k}\Omega$ ) and  $2\text{-}\mu\text{A max}$  leakage current (at 60 Hz, input-to-output, 240 Vrms applied). Figure 2 shows common-mode rejection as a function of frequency and source unbalance.

Dynamic specs include: full-signal bandwidth (10-volt output span) of 4 kHz at  $G = 1 \text{ V/V}$ , 400 Hz at  $G = 1,000$ ,  $0.1 \text{ V}/\mu\text{s}$  slew rate, and 2 ms settling time to 0.1% of a 10-V step ( $G = 1$ ). Two grades are available, "A" and "B", differing only in max nonlinearity (0.03%/0.015%) and max CMV (750 Vrms,  $\pm 1,000 \text{ V peak}/1,500 \text{ Vrms}$ ,  $\pm 2,000 \text{ V peak}$ ). Prices (100s) are \$32 and \$36 for "A" and "B", respectively.

In Figure 3, the input of the AD208 is configured for gains  $> 1 \text{ V/V}$ , with the op amp connected as a follower-with-gain. The 100-pF capacitor (for gains  $> 50 \text{ V/V}$ ) minimizes switching noise and nonlinearity. The 2-k $\Omega$  input resistor limits input current in the off condition and reduces overload recovery time.

The AD208 was designed by Jeffrey Greenwald at ADI's Industrial Products Division, Norwood, Mass.

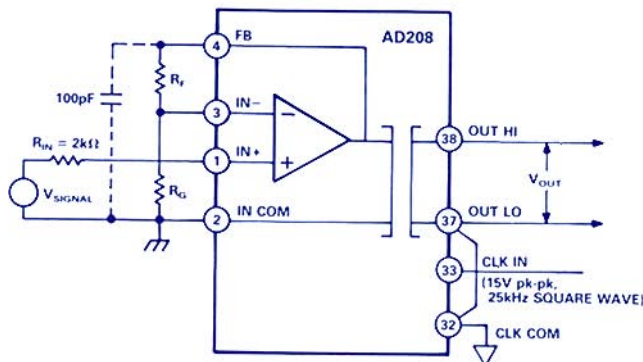


Figure 3. Input configuration for gains  $> 1 \text{ V/V}$ .

# COMPUTER INTERFACE PANEL HANDLES EIGHT ANALOG OUTPUTS

## STB-AOT interfaces RTI® and $\mu$ MAC® board families to field wiring

### Each channel has choice among four voltage- and two current ranges

The STB-AOT\* Analog Output Panel provides eight channels of non-isolated analog output via terminals for field wiring. The panel is compatible with the RTI-820, -220, -222, and -1266 bus interface boards, as well as the  $\mu$ MAC-6000, -1050, and  $\mu$ DCS-6000 family of data-acquisition/control subsystems (see *Analog Dialogues* 20-2, 23-3 and 23-4).

The interchangeable analog signal-conditioning panels in the STB family provide "mix and match" capability for isolated and non-isolated input and output, to/from a wide variety of actuators, recorders, and transducers. While providing different interface capabilities, all panel types in the family are addressed in the same format, transparent to the user's software.

The multiplexed interface between the STB-AOT and the computer-based subsystem it supports (in the RTI or  $\mu$ MAC family) minimizes the number of interconnection signal lines, reducing wiring and I/O costs while increasing flexibility (see the description of the RTI-220 and -222 on the facing page). For each channel, a choice among six analog output ranges is selectable by jumper:  $\pm 5$  V,  $\pm 10$  V, 0 to +5 V, 0 to +10 V, 0 to 20 mA, and 4 to 20 mA. Each channel has a dedicated sample/hold amplifier which holds the output value sent to it (when addressed) by the digital/analog converter on the host subsystem.

The update rate for each sample-hold depends on the host; the RTI-220 updates every 2.5 ms. Droop is 30  $\mu$ V/ms when voltage output is selected and 60 nA/ms for current output. Output accuracy is typically to within  $\pm 0.05\%$  of span. For current output, an on-board dc-dc converter supplies the output loop; its compliance ranges up to 10.5 V; if higher compliance voltage is needed, an external loop supply of from 18 to 32 volts increases compliance from 13 to 27 V (the external loop supply minus 5 V).



User field wiring is attached to the quick-disconnect screw connectors ranged along one edge of the STB-AOT. A single supply of +5 volts at 1.2 A is required (unless an external loop supply is also used); all other voltages required for analog output are developed within the STB-AOT. Two panels, each 8.25" wide  $\times$  6.8" high  $\times$  2.0" deep, can be mounted side-by-side in a standard 19" equipment rack. An optional cover provides protection for the panel circuitry and terminations, as well as space for function- and wiring labels. Price of the STB-AOT in small quantity is \$600.

*The STB-AOT was designed by Elissa Edelstein, of Analog Devices Industrial Products Division, Norwood, Massachusetts.*

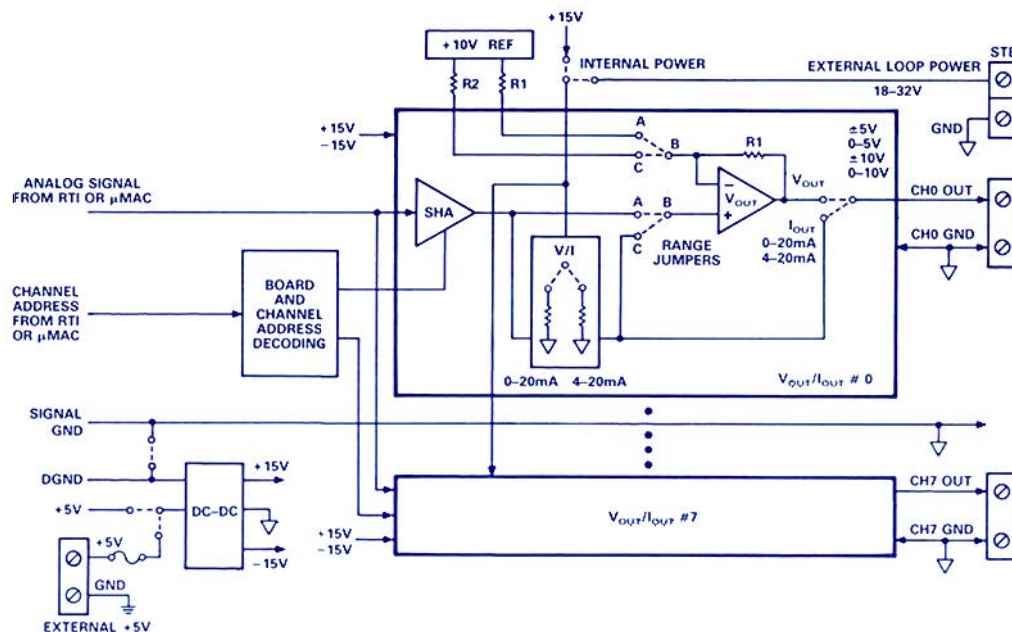


Figure 1. Block diagram of the STB-AOT, showing details of one channel.

\*Use the reply card for technical data.



# REAL-WORLD INTERFACE CARDS FOR MICRO CHANNEL SYSTEMS

RTI-220 & -222 support up to 64 analog inputs and 16 outputs (12 bits) for IBM PS/2; are compatible with 5B and STB signal conditioners

by Bob Eaton

The RTI-220\* and -222\* are plug-in analog input/output cards for Micro Channel systems, employed in IBM PS/2 Models 50, 60, 70, and 80—and fully equivalent personal computers. Both boards provide up to 16 analog outputs, and the RTI-220 I/O board, in addition, handles up to 64 analog input channels.

As Figure 1 shows, the RTI-220 has a single a/d converter with logic to keep track of 64 analog input channels multiplexed on the analog input bus and—like the RTI-222—a single d/a converter with 16 output channels multiplexed on its output bus. This type of multiplexing architecture provides high channel capacity at low cost-per-channel and permits quite flexible signal conditioning.

A wide selection of signal-conditioning options are available for interfacing the analog input and output buses to real-world sensors and transducers. For example, the I/O may be conditioned by highly configurable 5B-type modules\* (*Analog Dialogue* 20-2, 1986), multiplexed via the 5B02 panel, as well as by a series of general- and special-purpose (e.g., Model STB-TC thermocouple) panels, which offer lower cost per point. The STB-AOT, opposite, exemplifies an analog output panel.

Micro Channel eliminates jumpers on the board. Options may instead be configured through POS (programmable option select, for registered options) or software drivers. An ADF (Adapter Description File) is furnished to support POS configuration.

The analog input circuitry consists of a 12-bit successive-approximation a/d converter, with a choice of 0-to-5 or  $\pm 5$ -volt input ranges. The card allows selection of one of 64 channels (using six external address lines), either input range, and a programmable delay time before allowing the next conversion to start (it holds off a conversion until the selected channel is ready to be read).

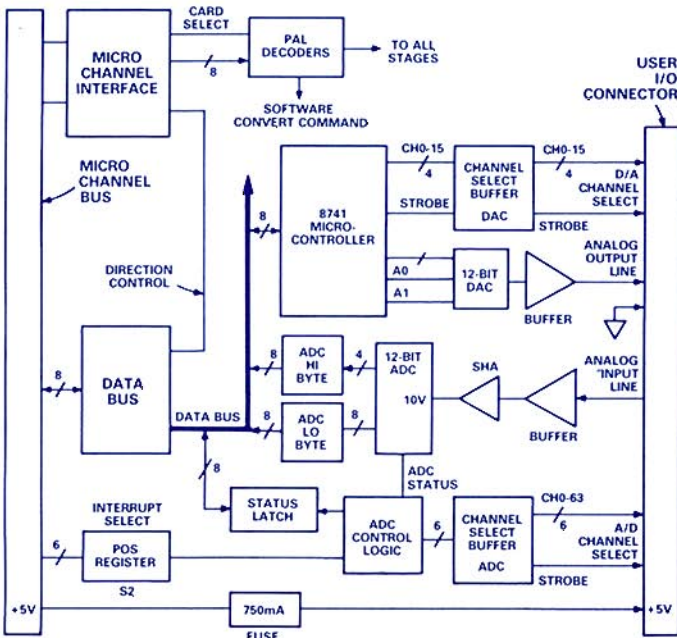
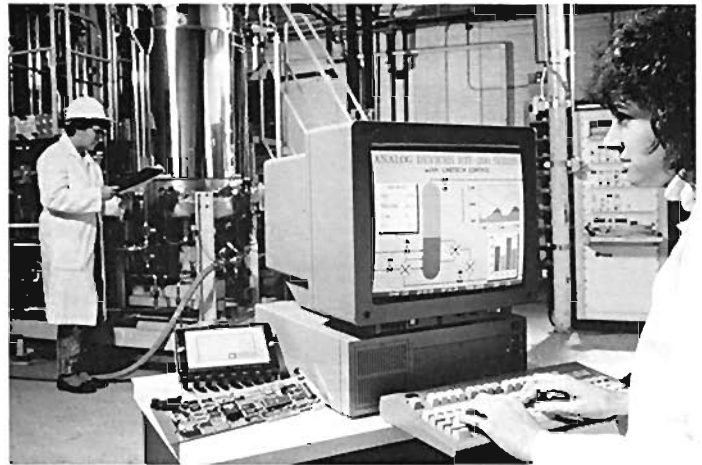


Figure 1. Block diagram of RTI-220.

\*Use the reply card for technical data.




The analog output circuitry uses a microcontroller to control the channel selection and update rates to the analog output modules or panels. The micro continuously updates the 16 analog outputs; each channel is updated every 32 ms. The 12-bit d/a converter's output range is  $\pm 5$  V. The interface panels and 5B modules permit the signal to be converted to a variety of voltage and current ranges for driving (for example) control valves, chart recorders, output transducers, and servomechanisms. The micro-computer controlling the analog outputs runs independently of the PS/2 system. If the PS/2 were not able to talk to the card or received a Reset, the outputs will continue to hold their present values. The outputs can be selected to power up at 0 or  $-5$  volts, even if the PS/2 was not able to boot up properly.

The boards are supported by software drivers in six popular languages running under PC DOS. Included are: IBM Interpreted BASIC, Microsoft Interpreted and Compiled BASIC, C, Quick-BASIC, and Borland International's TURBO Pascal. They are also supported by such application software as LABTECH NOTEBOOK, LT/CONTROL, Control EG, and THE FIX.

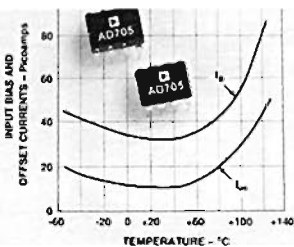
A Utilities disk, which contains an ADF, menu-driven software program (EXER200), and menu-driven calibration program (CAL220) accompanies each board. EXER200 can be used for debugging or to become familiar with the capabilities of the board prior to developing an application program. CAL220 allows the user to calibrate a board's analog I/O circuitry. Graphic representations of potentiometers to be adjusted are identified and displayed with a brief set of instructions; the graphics eliminates guesswork and guides users through simple calibration routines.

For real-world interfacing of isolated or non-isolated high-level, low-level, and preconditioned signals, the RTI-220 and -222 interface with Analog Devices 5B signal conditioners and I/O interface panels (TC, TCI, HLO2, HLI, and AOT) for direct connection to sensors and transducers. The RTI-220 and -222 are priced at \$650 and \$450 (single units).

At the Analog Devices Industrial Products Division, the design of the RTI-220 and RTI-222 was initiated by Steve Zella and completed by the author. Software drivers were designed by Ben Rogers. 

## PRECISION OP AMP

0.6  $\mu\text{V}/^\circ\text{C}$  max, 0.6  $\text{pA}/^\circ\text{C}$   
AD705's  $I_B$  is Only 100  $\text{pA}$  max



The AD705\* is a low-power low-cost operational amplifier with an exceptional combination of low offset voltage & drift and low bias current & drift. Specifically, the AD705T has 25  $\mu\text{V}$  max offset at +25 $^\circ\text{C}$ , 60  $\mu\text{V}$  max from -55 to +125 $^\circ\text{C}$ , and maximum drift of 0.6  $\mu\text{V}/^\circ\text{C}$ ; yet maximum  $I_B$  is only 100  $\text{pA}$ , 250  $\text{pA}$  over temperature (0.6  $\text{pA}/^\circ\text{C}$  max).

Such performance, useful in low-frequency active filters, precision integrators and other instrumentation, is not achievable with FET inputs; they tend to have significantly higher offset, drift, and voltage noise than the best of bipolar. Their bias current is low initially, but doubles (approximately) with each 10 $^\circ\text{C}$  temperature increase above 25 $^\circ\text{C}$  (1,000 $\times$  for a 100 $^\circ$  change).

Instead, bipolar technology is used, the input stage employs superbeta transistors for low bias current; this technology couples low bias current and drift with the already excellent voltage offset and drift found in devices like the AD707\* (*Dialogue* 22-1, p. 7). The AD705 directly replaces LT-1012 and OP-97 devices—and upgrades performance in applications for the ADOP-07, providing the same levels of performance with much higher source impedances, yet drawing only 1/6 as much supply current.

Minimum open-loop gain is 200  $\text{V/mV}$ , and the T grade has 114 dB minimum rejection of common-mode and power-supply. Unity-gain bandwidth is 800 kHz, slew rate is 0.15  $\text{V}/\mu\text{s}$ , and the device is capable of driving 10,000  $\text{pF}$  without instability.

The AD705 is available for all 3 temperature ranges and in various performance grades, packaged in 8-pin plastic mini-DIP, hermetic ceramic, and surface-mount (SOIC) packages. Prices start at 89¢ in 1000s. ▶

\*Use the reply card for technical data.

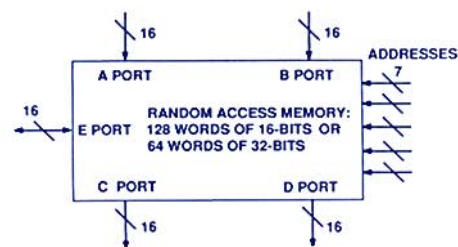
## REGISTER FILE HAS 5 16-BIT PORTS

Supports 40 MFLOPS microcoded DSP systems  
Configure it as 128 16-bit words or 64 32-bit words

The ADSP-3128A\* is a 5-port register file designed for temporary data storage in high-speed digital signal-processing (DSP) systems. It is a faster and otherwise improved version of the ADSP-3128, described in these pages in 1987 (21-1, p. 17).

With its five 16-bit ports—two for input, two for output, and one bidirectional, it is able to read or write twice per clock cycle on each port, in double-precision mode. It can store 128 16-bit words and is cascadable for increased word-length and/or storage depth. It readily supports 40-MFLOPS systems employing the floating-point ADSP-3212 multiplier and ADSP-3222 ALU in single- or double-precision computations.

With the above advantages, plus its flexible latching modes, the ADSP-3128A is configurable to address almost any high-performance multi-access data-storage



requirement. It makes possible heavily pipelined parallel microcoded architectures, which maximize system throughput. Typical applications include uses as a high-speed local data cache and crossbar data switch in high-performance microcoded processors and for crossbar data switching in multi-processing applications.

The ADSP-3128A, housed in a 144-pin grid array, is available in two grades for both the 0 to +70 $^\circ\text{C}$  (J,K) and -55 to +125 $^\circ\text{C}$  (S,T) temperature ranges; 883B versions of (S,T) are available. Prices (100s) start at \$145. ▶

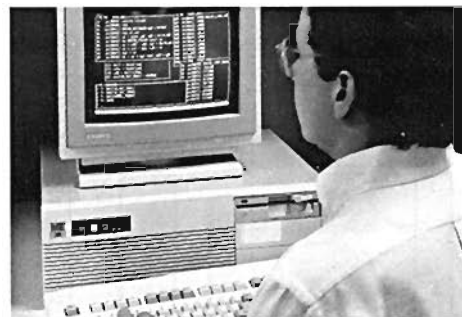
## SOFTWARE SUPPORT TOOLS FOR ADSP-2101

ADDS-2101-SW for DSP includes C compiler, System Builder, Assembler, Linker, PROM Splitter, Simulator

The ADDS-2101-SW\* is a set of software support tools for design and development of DSP systems using the ADSP-2101 and ADSP-2102 single-chip microcomputers. The software modules include System builder, Assembler, Linker, Simulator, C Compiler, and PROM splitter. The tools are useful in developing any system using these chips, as well as in evaluating them.

The *System builder* defines a hardware architecture. The *Assembler*, *Linker*, and *PROM splitter* prepare applications firmware for memory devices. The *Simulator* provides a means of system modeling and code development, allowing hardware and software development to proceed before prototypes are constructed. The *C compiler* translates C language files into ADSP-2101's clear, concise, and powerful assembly language, allowing development of applications software in a high-level language.

The ADSP-2101 Cross-Software Development System is currently available for



PC-DOS™ (IBM) and MS-DOS® (Microsoft). The ADSP-2101 *Cross-Software Manual*, supplied with the Cross Software, provides a complete programmer's reference to all directives, operation of each Cross Software module, and details of the ADSP-2101 assembly language. Consult Analog Devices about the availability of Cross Software on other platforms.

Available packages include an Assembly package (System Builder, Assembler, Linker, PROM Splitter), Simulator only, and a complete software package. ▶

## DIGITAL-TO-RESOLVER CONVERTERS

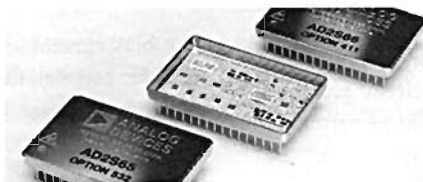
Hybrid AD2S65/66 for 14/16-bit resolution

Accuracy to  $\pm 1$  arc-min, dc autonulling optional

The AD2S65 and AD2S66\* are 14- and 16-bit digital-to-resolver converters (DRCs). They accept 14- or 16-bit binary words, representing angle ( $\theta$ ); and their output is a pair of sine- and cosine voltages, i.e., sinusoidal voltages  $90^\circ$  out of phase. The sine and cosine are amplitude modulated at the input reference frequency.

They are applicable in polar-to-rectangular coordinate conversion and axis rotation wherever resolvers are used for angular measurement and control: e.g., fire-control systems, simulation systems, automatic test equipment, PPI displays, etc. The 2S65/66 are ideal for testing *resolver to digital converters*, such as the 2S80.

Autonulled versions are available, with low dc offset ( $\pm 0.5$  mV typical,  $\pm 2.5$  mV maximum) over the full frequency- and operating temperature ranges. Low offset voltage



means that external trim adjustments are not required, particularly important in display and test applications.

The AD2S65/66, pin-compatible replacements for the DRC1765/66, are available in accuracy grades of  $\pm 1$ ,  $\pm 2$ , and  $\pm 4$  arc-min error; and radius error (transformation ratio) is only 0.03%—important in coordinate conversion and display applications, as well as simulation and test of RDCs. Both devices are housed in hermetically sealed welded metal packages, and are specified for 0 to  $+70^\circ\text{C}$  and  $-55$  to  $\pm 125^\circ\text{C}$  temperature ranges. Prices start at \$359 (1-9). ▶

## 50-MB/s DATA QUALIFIER FOR DISK DRIVES

Provides three levels of qualification:

Amplitude, time above threshold, and data polarity

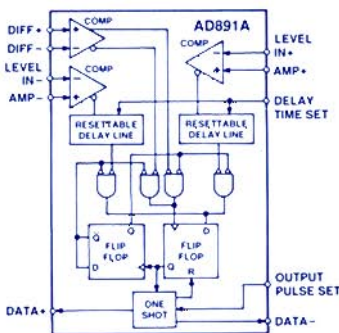
Was there a pulse, and when did it occur? The AD891A\* Data Qualifier, with its companion chip, the AD890 Wideband Channel Processor (*Analog Dialogue* 22-1, 1988, pp. 3-6), can recover binary information from differentiating channels with transfer rates exceeding 50 megabits per second. Like the more-basic AD891, the AD891A qualifies on amplitude; however, it also considers the additional criteria of *time above threshold* and *data polarity*.

A pair of comparators allows + & - swings of the incoming pre-conditioned signal to be compared against separate amplitude-qualification levels. The comparators drive NAND-gated flip-flops, via single-resistor-programmable resettable delay lines—by which the user can define the minimum time a data pulse must exceed the level before a zero-crossing can be ascertained.

A third comparator detects zero crossings out of an external differentiating network to

find signal peaks and initiate trials to determine validity and polarity. When a valid pulse has been identified, a time-domain-filter one-shot generates a pulse of single-resistor-programmable width. While the output is generated, the NAND-gated flip-flop is disabled to prevent the detection of additional zero-crossing events.

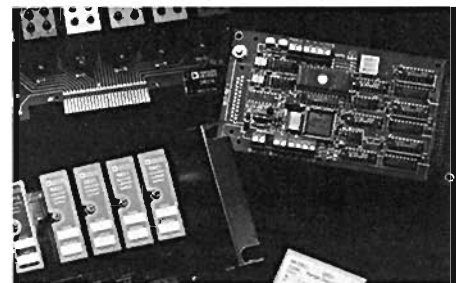
The temperature-compensated, 10 KH ECL-compatible AD891A is specified to operate over the 0 to  $+70^\circ\text{C}$  temperature range. It is housed in a 20-pin PLCC package. Prices start at \$4.12 (10,000s). ▶



\*Use the reply card for technical data.

## 6B50 DIGITAL I/O

24 input-or-output channels  
RS-232 to host, RS-485 to 6Bs



The 6B50\* is a digital input/output board that is compatible with the other members of the 6B Series (see *Analog Dialogue* 23-1, 1989, pp. 3-5) at the system level. Its real-world interface consists of 24 one-bit digital channels, which may be individually configured as inputs or outputs; at the other end, it can interface to other 6B-series backplanes via RS-485—or to a host via RS-232 (6B50-2). A serial-interface device, it has a command/response protocol similar to that of other 6B modules.

In response to a command from a host, it produces logic levels suitable for interfacing with industry-standard optoisolated digital I/O panels. All I/O channels can be configured for input or output, using bit (single-channel) or byte (groups of 8) addressing. It can be connected to opto-isolated solid-state relays, using (for example) a DB-16 or a DB-24 backplane and a standard 50-conductor cable. The status of the port can be read back by the host, to confirm the I/O configuration.

Typical applications are in remote monitoring and factory automation, as well as distributed data acquisition and control, industrial pilot-plant control, machine control, and energy management.

The 6B50 has an on-board microprocessor that communicates with the host to exchange command and status information. An EEPROM stores system parameters (address, baud rate, etc.) and I/O configuration information.

The 6B50 board profile is  $3.47" \times 6.5"$ . It requires a +5-volt supply ( $\pm 5\%$ ) at 225 mA quiescent plus external load current. It is designed to operate over a 0 to  $+70^\circ$  temperature range. Price in small quantity is \$220. (6B50-1). ▶

# Ask the Applications Engineer—6

by James Bryant

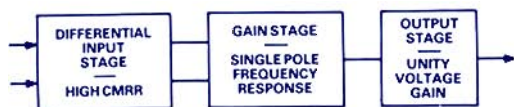
## OP-AMP ISSUES

**Q.** Why are there so many different types of operational amplifier?

**A.** Because there are so many parameters that are important in different applications, and because it is impossible to optimize all of them at once. Op amps may be selected for speed, for noise (voltage, current or both), for input offset voltage and drift, for bias current and its drift, and for common-mode range. Other factors might include power: output, dissipation, or supply, ambient temperature ranges, and packaging. Different circuit architectures and manufacturing processes optimize different performance parameters.

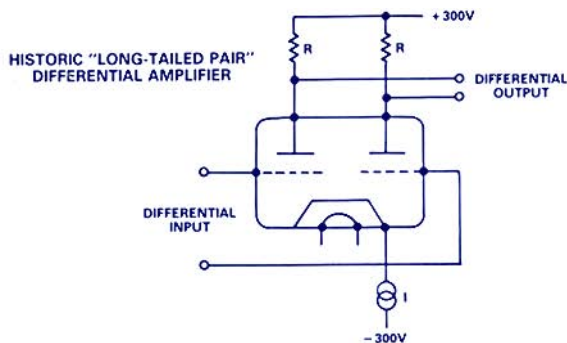
**Q.** Is there any common factor in the design of op-amps?

**A.** Yes—most classical (voltage input) op-amps are three-stage devices, consisting of an input stage with differential input and differential output—with good common-mode rejection—followed by a differential-input, single-ended output stage having high voltage-gain and (generally) a single-pole frequency response; and, finally, an output stage, which usually has unity voltage gain.

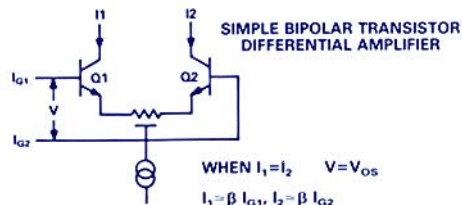


**Q.** So where are the differences?

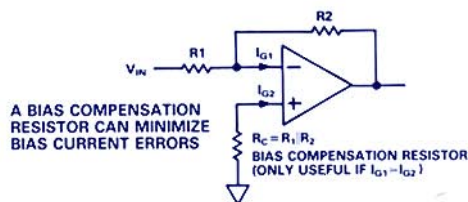
**A.** There are many possible variations on this basic design. One of the most fundamental is the structure of the input stage. This stage is almost always a long-tailed pair—that is to say, a pair of amplifying devices connected as in the figure—but the choice of devices has a profound effect on the input parameters of the op amp. The figure was drawn with thermionic tubes to avoid any suggestion of partiality in favour of any particular semiconductor device. Since thermionic devices at present are not generally available in IC chip form, a monolithic op-amp will have an input stage built with bipolar or field-effect transistors.



A long-tailed pair built with bipolar transistors is shown in the next figure. Its strong features are its low noise and, with suitable trimming, low voltage offset. Furthermore, if such a stage is trimmed for minimum offset voltage it will inherently have minimum offset drift. Its main disadvantage stems from the proportionality of the emitter and base currents of the transistors; if the emitter current is large enough for the stage to have a reasonable bandwidth, the base current—and hence the bias current—will be relatively large (50 to 1,000 nA in general-purpose op-amps, as much as 10  $\mu$ A in high-speed ones).

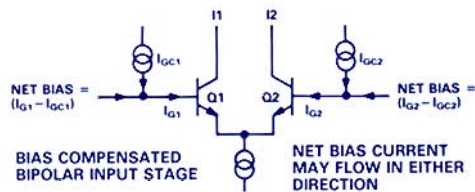


The bias currents in the inverting and non-inverting inputs are unipolar and well matched (their difference is called *offset current*), and they decrease in a minor way with increasing temperature. In many applications, the accurate matching may be used to compensate for their high absolute value. This figure shows a bias compensation circuit where the bias current in the non-inverting input flows in  $R_c$  (known as the bias compensation resistor); this compensates for the voltage drop as the bias current in the inverting input flows through  $R_2$ .  $R_c$  is made nominally equal to the parallel combination of  $R_1$  and  $R_2$ .—it can be trimmed to minimize error due to non-zero offset current).



Such bias compensation is only useful when the bias currents are well-matched. If they are not well-matched, a bias compensation resistor may actually *introduce* error.

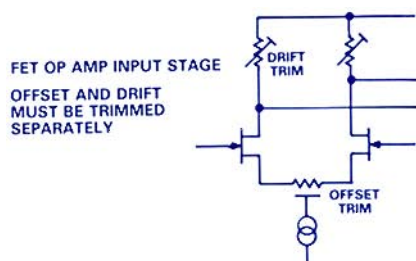
If a bipolar input stage is required without the drawback of such a high bias current, a different form of bias compensation may be used by the chip designer (next figure). The same long-tailed pair is used, but the major portion of the current required by each base is supplied by a current generator on the chip. This can reduce the external bias current to 10 nA or less without affecting the offset, temperature drift, bandwidth or voltage noise. Bias current variation with temperature is quite low.



There are two disadvantages to such an architecture: the current noise is increased and the external bias currents are not well matched (indeed, they may actually flow in opposite directions, or change polarity as chip temperature changes). For many applications these features are no drawback; indeed, one of the most popular low-offset op-amp architectures, the OP-07, uses just such an architecture, as do the OP-27, OP-37 and the AD707, which has a guaranteed offset voltage of only 15  $\mu$ V. Bias-compensated amplifiers of this type are often recognizable when their data sheets explicitly specify *bipolar* bias current, for example,  $\pm 4.0$  nA.

Where bias currents of even a few nanoamps are intolerable, bipolar transistors are usually replaced by field-effect devices. In the past, MOSFETs have been somewhat noisy for op-amp input

stages, although modern processing techniques are overcoming this drawback. Since MOSFETs also tend to have relatively high offset voltages, *junction* FETs (JFETs) are used for high-performance low-bias-current op amps. A typical JFET op-amp input stage is shown in this figure.



The bias current of a JFET bears no relationship to the current flowing in the device, so even a wideband JFET amplifier may have a very low bias current—values of a few tens of picoamperes are commonplace, and the AD549 has a guaranteed bias current of less than 60 fA (one electron per three microseconds!) at room temperature.

The qualification “at room temperature” is critical—the bias current of a JFET is the reverse leakage current of its gate diode, and the reverse leakage current of silicon diodes approximately doubles with every 10°C temperature rise. The bias current of a JFET op-amp is thus not stable with temperature. Indeed, between 25°C and 125°C, the bias current of a JFET op-amp increases by a factor of over 1,000. (The same law applies to MOSFET amplifiers, because the bias current of most MOSFET amplifiers is the leakage current of their gate-protection diodes.)

The offset voltage of a JFET amplifier may be trimmed during manufacture, but minimum offset does not necessarily correspond to minimum temperature drift. It has therefore been necessary to trim offset and drift separately in JFET op-amps, which results in somewhat larger values of voltage offset and drift than are available from the best bipolar amplifiers (values of 250  $\mu$ V and 5  $\mu$ V/°C are typical of the best JFET op-amps). Recent studies at Analog Devices, however, have resulted in a patented trimming method which is expected to yield much better values in the next generation of JFET op-amps.

We thus see that there are trade-offs between offset voltage, offset drift, bias current, bias current temperature variation, and noise in operational amplifiers—and that different architectures optimize different features. The table compares the features of the three commonest op-amp architectures. We should note one more category, typified by the new AD705 (introduced briefly on page 18), using bipolar *superbeta* input transistors; it *combines low offset voltage and drift with low bias current and drift*.

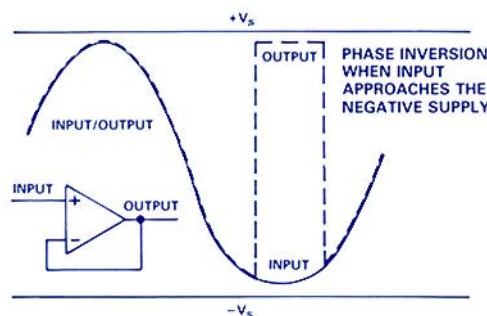
CHARACTERISTICS OF OP-AMP INPUT STAGES

	SIMPLE BIPOLAR	BIAS-COMPENSATED BIPOLAR	FET
OFFSET VOLTAGE	LOW	LOW	MEDIUM
OFFSET/DRIFT	LOW	LOW	MEDIUM
BIAS CURRENT	HIGH	MEDIUM	LOW-VERY LOW
BIAS MATCH	EXCELLENT	POOR (CURRENT CAN BE IN OPPOSITE DIRECTIONS)	FAIR
BIAS/TEMP VARIATION	LOW	LOW	BIAS DOUBLES FOR EVERY 10°C RISE
NOISE	LOW	LOW	FAIR

Q. What other features of op amps should the user know about?

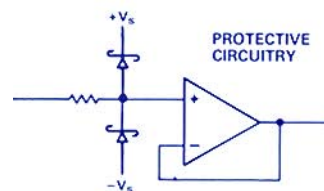
A A common problem encountered with JFET op-amps is phase inversion. If the input common-mode voltage of a JFET op-amp approaches the negative supply too closely, the inverting and

non-inverting input terminals reverse functions. Negative feedback becomes positive feedback and the circuit may latch up. This latchup is unlikely to be destructive, but power may have to be switched off to correct it. This figure shows the effect of such phase inversion in a circuit where latch-up does not occur. The problem may be avoided by using bipolar amplifiers, or by restricting the common-mode range of the signal in some way.



A more serious form of latchup can occur in both bipolar and JFET op-amps if the input signal becomes more positive or negative than the respective op-amp power supplies. If the input terminals go more positive than  $+V_s + 0.7$  V or more negative than  $-V_s - 0.7$  V, current may flow in diodes which are normally biased *off*. This in turn may turn on thyristors (SCRs) formed by some of the diffusions in the op-amp, short-circuiting the power supplies and destroying the device.

To avoid such destructive latch-up it is important to prevent the input terminals of op-amps from ever exceeding the power supplies. This can have important implications during device turn-on: if a signal is applied to an op-amp before it is powered it may be destroyed at once when power is applied. Whenever there is a risk, either of signals exceeding the voltages on the supplies, or of signals being present prior to power-up of the op-amp, the terminals at risk should be clamped with diodes (preferably fast low-forward-voltage Schottky diodes) to prevent latchup from occurring. Current-limiting resistors may also be needed to prevent the diode current from becoming excessive (see the figure).



This protection circuitry can cause problems of its own. Leakage current in the diode(s) may affect the error budget of the circuit (and if glass-encapsulated diodes are used, their leakage current may be modulated at 100 or 120 Hz due to photoelectric effects if exposed to fluorescent ambient lighting, thus contributing *hum* as well as dc leakage current); Johnson noise in the current-limiting resistor may worsen the circuit's noise performance; and bias current flowing in the resistor may produce an apparent increase in offset voltage. All these effects must be considered when designing such protection.

The important subjects of noise, interference, bypassing, and grounding demand discussion—but we're out of space! We'll come back to them again in future chats; meanwhile you may want to take a look at some of the references in the footnotes on page 7 of Analog Dialogue 23-3. ▣

# Worth Reading

## APPLICATION NOTES\*

**AD7672 converter delivers 12-bit 200-kHz sampling systems**, by John Reidy (8 pages). Shows how to build a 200-kHz sampling ADC system that maintains 12-bit performance for full-power signals up to 75 kHz. The ADC is the 12-bit, 3- $\mu$ s AD7672, used with a discrete sample-and-hold design.

**Asynchronous clock interfacing with the AD7878**, by John Reidy (2 pages). The AD7878 (*Analog Dialogue* 22-2, page 21) is a fast, complete 12-bit a/d converter with a versatile 8-word FIFO DSP interface. Its data sheet shows ways of interfacing *synchronously*, using the processor's clock. This Application Note shows how to interface *asynchronously* to such processors as the ADSP-2100A, TMS320C25, and DSP56000, using an external clock, when synchronous interfacing is either not possible or not desirable.

**Bandwidth, OFF isolation, and crosstalk performance of the ADG5XXA multiplexer series**, by Dan Sheehan and Matt Smith (6 pages). The ADG5XXA multiplexer series is a family of single 8/16-channel and dual 4/8-channel latched and unlatched CMOS multiplexers (*Analog Dialogue* 22-1, 1988, pp. 16-17). This application note attempts to answer the most-frequently asked questions concerning crosstalk, isolation, and bandwidth; results described include bandwidths in excess of 40 MHz with isolation better than 60 dB at that frequency.

**FIFO operation and boundary conditions in the AD1332 and AD1334**, by Stephan Goldstein (2 pages). The AD1332/4 are 12-bit 1- and 4-channel sampling a/d converters that contain 32-word FIFOs. This Application Note provides additional detail (beyond the data sheet) about timing, overflow, underflow, and generation of interrupts when the FIFO is used.


**Simultaneous and independent sampling of analog signals with the AD1334**, by Stephan Goldstein (4 pages). This Application Note supplements and clarifies the data sheet's description of these operating modes. As a bonus, Figures 1 and 2 correct slight errors in the handling of the Sample inputs in Figures 15 and 16 of the first printing of the data sheet.

**Implement infinite sample-and-hold circuits using analog input/output ports**, by Mike Byrne (4 pages). Zero-droop or infinite sample-and-hold? However you describe it, the function is clear. And it's easily implemented on monolithic I/O ports—devices that independently combine at least one ADC and one DAC. Such a circuit was described on the AD7569 data sheet. Here now are descriptions of single- and dual-channel infinite sample-holds using the AD7569, AD7669, and AD7769.

**Using the 2S80 Resolver-to-Digital Converters with synchros: solid-state Scott-T circuit**, by Mark Schirmer (4 pages). This Application Note describes a simple circuit that can be used to interface synchros to the 2S80 family of monolithic resolver-to-digital converters. The solid-state Scott-T discussed here is a viable alternative to the larger and more-costly transformers that are usually employed for format conversion.

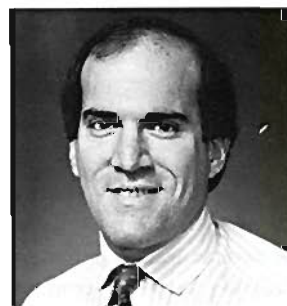
## SERIAL PUBLICATION

**DSPatch®—The Digital Signal-Processing Applications Newsletter**, Number Fourteen (winter, 1989) is now available, with 20

pages (up 25% from previous issues). This issue features the ADSP-3212/22 chipset and the ADSP-3128A Register File (briefly described here on page 18). Also included are two stories describing customer applications: the MAST (multiprocessor array space technology) computer, a high-performance computer from SCI Technology, Inc., currently in use at NASA and scheduled to be used on board a future Space Shuttle flight; and the Ketema Model 5400 Underwater Telephone. "How to talk analog" begins a series on sigma-delta conversion technology, and a useful Applications piece describes the nitty-gritty details of booting the ADSP-2101 one byte at a time. In addition there are the usual informative columns on product and program status. 

## MORE AUTHORS (Continued from page 2)

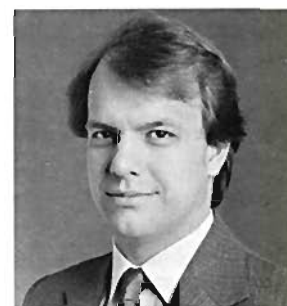
**Bob Fine** (page 9) is Applications Engineering Manager for the DSP division at Analog Devices. After graduation with a BSEE from Northeastern University in 1979, he joined Analog Devices as an analog designer of board-level products for measurement and control. Since he joined the DSP division in 1982, he has been working on applications projects. He now manages the Applications group, which provides training, publishes application notes, and assists customers in the uses of ADI's DSP products.




**David Fair** (page 9) is ASIC Marketing Manager of Analog Devices Semiconductor's Converter Operating Group. Previously he was the Product Marketing Manager of ADI's Digital Signal Processing Division. He has a PhD in the Philosophy of Science from Princeton and a BA in Physics from Pomona College. His interests include bicycling, digital audio, and (belatedly) fatherhood.



**Bob Eaton** (page 17) is an Engineer Assistant in the Subsystems Design Group of the Industrial Products Division, Norwood, Massachusetts. In his more than five years at ADI, he has served in Systems Support Engineering and in Subsystems Design. He is approaching completion of a BSEE program at Northeastern University and has an AS in Horticulture. He enjoys reading, gardening, and woodworking.



**James Bryant** (page 20) is European Applications Manager for Analog Devices, based in Newbury, England. His photo and a biographical sketch appear in *Analog Dialogue* 23-2.

**Cover design:** The front-cover pictorial of this issue of *Analog Dialogue*—and of many previous issues—was designed and executed by Shelley Cohane, of Design Encounters, Hingham, Massachusetts. 

\*Use the reply card to request Application Notes and DSPatch.

An Eclectic Collection of Miscellaneous Items of Timely and Topical Interest. Further Information on Products Mentioned Here May Be Obtained Via the Reply Card.

## IN THE LAST ISSUE

Volume 23, Number 4, 1989, 24 Pages

Editor's Notes, Authors

*Pin Electronics for High-Speed Automatic Testing* (AD1315/21/22)  
*12-Bit DACs Optimized for Direct Digital Synthesis* (AD9712/13)  
*8-Bit Dual Analog I/O Port for Position Monitoring & Control* (AD7769)  
*Floating-Point Data-Acquisition System* (AD1330)  
*Distributed Data Acquisition & Control with Flexibility* ( $\mu$ MAC-1050)  
*High-Performance Electrometer Op Amp in 8-Pin Plastic DIP* (AD546K)  
*Industry's Fastest Monolithic FET-Input Op Amp* (AD843)  
*Complete Monolithic 12-Bit DAC Interfaces with Fast DSPs* (AD7848)  
*Monolithic Dual 12-Bit DAC/PORTs Save Space, Power, Cost* (AD7237/47)  
*Fast Precision Comparator Has Wide Differential Input Range* (AD790)  
*Ultrafast Single and Dual TTL-Compatible Comparators* (AD9696/98)  
 New-Product Briefs:  
 PWM Test Boards Enhance Mixed-Signal Bench Test System (LTS)  
 Fast Precision FET-Input Dual Op Amp (AD746 = 2  $\times$  AD744)  
 Monolithic Cold-Junction Compensator for 1B51 (AC1226)  
 Updating the Disk Selection Guide  
 Ask the Applications Engineer—5: *Comparator Problems*  
 Worth Reading, More Authors  
 Potpourri (Last Issue, Errata, Product Notes, Updates, Patents)  
 Advertisement

**ERRATA:** . . . AD9020 & AD9060 data sheets: page 2, ENOB at 10.3 MHz should be 8.0; page 5, add pin numbers 66 & 67 in the column labeled Pin No., opposite GROUND . . . AD9060 data sheet: page 5, pin 52 is a ground connection only; it is not connected to +V<sub>s</sub> . . . AD9617 data sheet: at top of page 8, R<sub>f</sub> should be 400  $\Omega$ , not 400 k $\Omega$  . . . AD9696/98 data sheet: page 2, Input Bias Current max at 25°C should be 55, not 35; max over temperature should be 110, not 70; page 3, Negative Supply Current (-5.2 V) max for AD9696 should be 4.0, not 3.0 (both columns); max for AD9698 should be 8.0, not 6.0 (both columns) . . . For these fixed-point DSP products, the most-correct information is in the DSP Products Databook; discard loose data sheets: ADSP-1008A, -1009A, -1010A, -1012A, -1060A, -1080A, -1081A.

**TIMELY TOPICS:** . . . Come see us at these shows during 1990: IEEE ICASSP in Albuquerque, NM, April 3-6; IEEE CICC/90 in Boston, May 13-16; Siggraph '90 in Dallas, August 6-10; ISA '90 in New Orleans, October 14-19; Electronic Imaging '90 in Boston, October 30-November 1 . . . Three-day Analog Devices workshops on the ADSP-2100 Family of single chip Digital Signal Processors will be held in Massachusetts, June 6-8, and in California, June 12-14, 1990. For information, CWYLSO.\* Or for information about the workshops and much more, log onto the DSP Bulletin Board, (617) 461-4258 (8 data bits, 1 stop bit, no parity, 300/1200/2400 baud).

**PRODUCT NOTES:** . . . The ADSP-2101 free Simulator Demonstration disk is now available in a 360-kilobyte double-sided double-density 5 1/4" disk, as well as the original 1.2-megabyte disk. CWYLSO\* . . . The  $\mu$ MAC-1050 (see the last issue) can now be used with LABTECH NOTEBOOK and LABTECH CONTROL, from Laboratory Technologies. CWYLSO\* . . . The AD9005 12-bit, 10-MSPS a/d converter is now available in a significantly lower-cost "J" version with slightly higher differential nonlinearity and just 1 dB more of harmonic distortion. CWYLSO\* . . . The venerable AD569 16-bit IC DAC (ANALOG DIALOGUE 20-2, 1986) is available in a variety of package alternatives, including plastic and hermetic cavities and through-hole and surface-mount technologies. It's also available in an 883B version. CWYLSO\* . . . The RTI-800 Series DOS Drivers have been enhanced in several ways: they now support Borland International Turbo C (Rev. 2.0) and TURBO Pascal Rev. 5.5; and the RTI-820 calibration program supports the STB-AOT Analog Output Panel. CWYLSO\* . . . All new AD1175 22-bit ADCs are now calibrated to the new international standard volt that became effective 1 January, 1990 . . . The AD1362 replaces the AD362 directly in most applications, with improved performance (it is also used as the analog input section in the AD363R and AD364R). However, it is sensitive to power-supply sequencing, and a destructive latchup condition can occur if the +5-volt supply is turned on ahead of the +15-volt supply. Simple protection strategies exist; for help, call Applications Engineering at ADI's Microelectronics Division (508) 657-7960. Also, as with most CMOS circuitry, unused input channels should be connected "somewhere," usually to ground, to provide a return path for leakage currents. Incidentally, for stable 5.12-V and 10.24-V scale factors, you should interpose a fixed attenuator and follower, rather than adding series input resistance (CWYLSO\*) . . . The 16-bit, 50-kHz AD1380's sample-and-hold has an input impedance of 4 k $\Omega$  ( $\pm$ 20%). If a buffer is needed, the AD711 op amp works quite well! . . . For the 12-bit AD1332 and AD1334 sampling ADCs, allow  $\geq$ 17 clock periods after the trailing edge of the RESET signal before starting a new conversion (CWYLSO\*) . . . Improved specs: the AD1856 and AD1860 16- and 18-bit audio DACs now dissipate only 110 mW typical, 150 mW max (40% and 57% less than some other devices that might be considered) . . . More and more products (including more than 100 CMOS converter families) have commercial versions available in PIGC and SOIC and/or are available in tape- & reel packaging. CWYLSO\* . . .

**MILITARY ROLL CALL:** . . . The ADSP-1010R 16  $\times$  16-bit fast multiplier/accumulator (ANALOG DIALOGUE 23-2) can now be ordered against Standard Military Drawing (SMD) 5962-88733 in DIPs and PGAs with 55-, 65-, and 75-ns speed grades . . . The AD2701 -10-volt Reference is available with either standard 883B screening (data sheet available) or to SMD 5962-85030 . . . The innovative and highly accurate AD598 LVDT/RVDT monolithic signal conditioner (ANALOG DIALOGUE 23-3) is now available with processing conforming to 883B (data sheet available) . . . Radiation test information (RADTEST<sup>SM</sup> Data Service) is available in brief summary form for each of nearly 100 products. CWYLSO\* . . . The AD2880 series of monolithic resolver-to-digital converter includes units screened to 883B in two package options, a 40-pin ceramic DIL and a 44-contact LCC . . . Military surface-mount applications now served by the commercial-only 2582 can use the AD2880SE883B and the AD2880TE883B (LCCs); those packages have the same pinout as the 2582, but with no VCO output (pin 41 is a no-connect).

**PATENTS RECEIVED** . . . 4,791,318 to Stephen Lewis and Scott Lefton for MOS Threshold Control Circuit . . . 4,855,618 to A. Paul Brokaw for MOS Current Mirror with High Output Impedance and Compliance . . . 4,862,073 to Jeff Barrow for Repetitive Wave Sampler . . . 4,864,454 to Ed Wolfe for Means for Reducing Damage from Electrostatic Discharge . . . 4,866,505 to Carl Roberts for Aluminum-Backed Wafer and Chip . . . 4,878,770 to Paul Ruggerio and Cynthia Anderson for IC Chips with Self-Aligned Thin-Film Resistors . . . 4,879,505 to Jeff Barrow and A. Paul Brokaw for Temperature and Power-Supply Compensation Circuit for Integrated Circuit . . . 4,884,075 to Christopher Mangelsohn for Decoding Circuit for Flash-Type Analog-to-Digital Converter . . . 4,885,585 to Jeff Barrow and A. Paul Brokaw for Ramp Generator Reset Circuit.

\*CWYLSO = Check with your local sales office . . . Trademarks in this issue:  $\mu$ MAC<sup>®</sup>, RTI<sup>®</sup>, DSPatch<sup>®</sup>: Analog Devices, Inc. • IBM, Micro Channel, PS/2, PC, PC DOS: International Business Machines Corporation • THE FIX: Intellution, Inc. • MS-DOS, Microsoft, QuickBASIC: Microsoft Corporation • TURBO Pascal: Borland International Corp. • Control EG: Quinn-Curtis • LABTECH NOTEBOOK, LT/Control: Laboratory Technologies Corporation.

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